

Final Report for DOE/EERE

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EXECUTIVE SUMMARY

1366 Technologies' Project Silicon addresses two of the major goals of the DOE's PV Manufacturing Initiative Part 2 program: 1) How to reclaim a strong silicon PV manufacturing presence and; 2) How to lower the levelized cost of electricity ("LCOE") for solar to \$0.05-\$0.07/kWh, enabling wide-scale U.S. market adoption. To achieve these two goals, US companies must commercialize disruptive, high-value technologies that are capable of rapid scaling, defensible from foreign competition, and suited for US manufacturing. These are the aims of 1366 Technologies Direct Wafer™ process.

The research conducted during Project Silicon led to the first industrial scaling of 1366's Direct Wafer™ process – an innovative, US-friendly (efficient, low-labor content) manufacturing process that destroys the main cost barrier limiting silicon PV cost-reductions: the 35-year-old grand challenge of making quality wafers (40% of the cost of modules) without the cost and waste of sawing. The SunPath program made it possible for 1366 Technologies to build its demonstration factory, a key and critical step in the Company's evolution. The demonstration factory allowed 1366 to build every step of the process flow at production size, eliminating potential risk and ensuring the success of the Company's subsequent scaling for a 1 GW factory to be constructed in Western New York in 2016 and 2017. Moreover, the commercial viability of the Direct Wafer process and its resulting wafers were established as 1366 formed key strategic partnerships, gained entry into the \$8B/year multi-Si wafer market, and installed modules featuring Direct Wafer products – the veritable proving grounds for the technology.

The program also contributed to the development of three Generation 3 Direct Wafer furnaces. These furnaces are the platform for copying intelligently and preparing our supply chain – large-scale expansion will not require a bigger machine but more machines. SunPath filled the crucial development step between the original research effort in Lexington and the GW factory scheduled to be online before the end of the decade.

At the conclusion of the project, it is clear that the Direct Wafer™ technology will have a dramatic impact on the entire silicon photovoltaic supply chain by effectively doubling existing silicon capacity (by reducing silicon usage by 50%) and reducing supply chain capital costs by 35%. The technology, when fully-scaled in the US, will also lead to significant job growth, with the eventual creation of 1,000 jobs in Western New York.

COMPARISON OF PROPOSED VERSUS ACTUAL PROJECT GOALS

The following table summarizes the project's proposed goals versus actual progress for each task. Deviations between an Initial negotiated deliverables / milestones and an actual deliverable / milestone are discussed in the "Deliverable / Milestone Deviations" section of the Technical Narrative.

Task #	Task description	Initial Negotiated Deliverable / Milestone	Actual Deliverable / Milestone
1.0	Module Production and Qualification	Deliver 5 modules, 50 wafers and 25 cells >15% efficiency to DOE	First 5 modules delivered Dec 2012 and installed at NREL test site.
2.0	Production Facility Renovation and Move	Move operations	Moved from 16k sq.ft. lab in Lexington to 42k sq. ft. facility in Bedford with dedicated production space.
3.0	Build and Operation of Furnaces 1 and 2	PO's placed for Production Furnace and Components	Completed
		Initial production furnaces commissioned. Deliver 100 wafers grown	Completed
		Meet furnace operating metrics (1000 wafers/day, eff > 15%)	Completed
4.0	Business Goals to Support Expansion to 40MW/yr	Economics Report to validate adjusted COGS of \$0.25/W	More aggressive target of <\$0.20/W set based on market conditions
			Installed texturing equipment
5.0	Prepare for Additional Capacity	Manufacture of five 60 cell modules, > 223W each	Completed. First modules rated 240-245W
		Deliver data for 100 representative wafers < 60um TTV, 2500 cells > 15.5% eff made by customer	Geometry targets demonstrated. Increased target efficiency to >16.0% and completed.
6.0	Furnace Build-Out	Additional furnaces 3-5 installed, > 1000 wafers grown. 100 sample cells > 16.5%	Completed
		10kW of Modules installed by customer w/ performance data	Completed (7.5kW in Japan, 2.5kW in Germany)
7.0	Operations and Evaluation of Full Set of Production Furnaces	Install 60 kW of modules at customer site	Installed 50kW of modules at General Electric in Schenectady, NY
		Adjusted COGS Test <\$0.25/W. Data of 40kW averaging >16.0%	Furnace operating metrics demonstrated Adjusted COGS <\$0.19/W. Wafers processed into >40kW cells averaging 18.3% efficiency
		Signed sales contracts for 40MW of Direct Wafer production in the US	Signed strategic partnership with Hanwha Q Cells which also fulfilled 40 MW sales contract requirement

PROJECT OBJECTIVE

For decades the industry standard process for manufacturing silicon (Si) wafers for solar cells (the most dominant photovoltaic (PV) technology) has relied on the formation of large ingots of multicrystalline silicon. Half of this valuable product is subsequently wasted as kerf when the ingots are sawn into wafers, which is a great expense.

The goal of this project is the first industrial scaling of 1366 Technologies' (herein after referred to as "1366") Direct Wafer process – an innovative manufacturing process that addresses the main barrier limiting silicon PV cost-reductions. The main barrier is the 35-year-old grand challenge of making quality wafers, which is 50% of the cost of modules, without the cost and waste of sawing. This simple, scalable process will allow 1366 to deliver "drop-in" replacement multicrystalline wafers ("multi-Si wafers") at 50% of the cost, 60% of the capital, and 30% of the electricity of conventional ingot casting and brick sawing manufacturing processes.

Objectives

At the end of the project, 1366 expected to achieve the following:

- Successfully build and operate a 40 megawatt (MW) Direct Wafer production plant.
- Secure customers for the initial Demo Direct Wafer™ factory and the subsequent gigawatt (GW) expansion through sampling.
- Establish and qualify supply chain relationships with raw material suppliers, equipment vendors, and customers to position for rapid expansion to >1GW within 2 years of project completion.
- Raise approximately \$20 Million in financing to allow for a large-plant build in the US.

PROJECT OUTCOMES

Task 1: Module Production and Qualification

Production of photovoltaic modules incorporating Direct Wafer products was the first major thrust of the SunPath project. Wafers were produced from our Demonstration Furnace, which at the time was capable of producing ~100 wafers per day. Cell processing was done partially using 1366's pilot cell line, but the majority of cell processing was done by University of Konstanz in Germany on a tolling basis. The solar cells were then assembled into modules by Spire Solar, a module equipment manufacturer located nearby to 1366 in their development lab. The first set of 5 modules were small, 24 cell modules as shown in Figure 1 below, with the 1366 Technologies team standing in front of our old facility at Hartwell Ave in Lexington. These modules were delivered to NREL for evaluation and testing.



Figure 1: First photovoltaic modules produced using Direct Wafers™, with 1366 team in front of 45 Hartwell Ave, Lexington prior to company move to Bedford.

NREL measurements of temperature coefficients showed similar characteristics to commercial silicon module of $-0.50\%/^{\circ}\text{C}$. Measurement of LID is summarized in Figure 2, Two of the modules were exposed to light outdoors and measured on two simulators before and after light exposure. The measurements before and after light exposure were within the uncertainty of the measurement, and measured power loss of 0.25% is within target range.

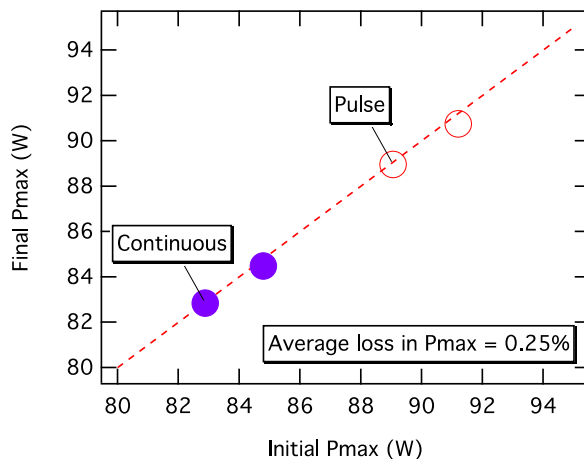


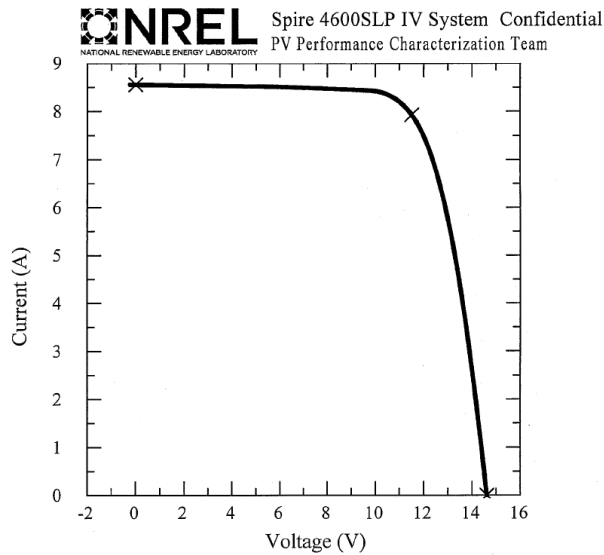
Figure 2: Comparison of maximum-power before and after light exposure outdoors.

Following the initial build of 5 small test modules, an industry standard size of 60 cells was fabricated using similar tolling and this was displayed at the Grand Opening celebration for our Bedford facility on January 30th, 2013. Customers eventually

conducted their own qualifications of modules they produced themselves using Direct Wafer products, but this early testing provided useful early validation.

**1366/Spire
multi-Si module**

Device ID: atc20120030_112712002 Device Temperature = 24.9°C
Dec 19, 2012 13:36:57 MT Device Area = 6214.6 cm²
Spectrum: ASTM G173 global Irradiance = 1000.0 W/m²



$V_{oc} = 14.61 \text{ V}$ $V_{max} = 11.50 \text{ V}$
 $I_{sc} = 8.553 \text{ A}$ $I_{max} = 7.928 \text{ A}$
Fill Factor = 73.0% $P_{max} = 91.20 \text{ W}$

Figure 3: NREL measurements of one of the 24 cell modules delivered in Dec 2012, with Pmax at the module level of 3.8 W per cell or 15.6%.

Task 2: Production Facility Renovation and Move

1366 moved operations into an existing 41,071 sq. ft. industrial building at 6 Preston Court in Bedford MA. In Q3-2012, design and engineering work was completed using a lead architect, engineering consultants and a general contractor to develop full construction documents and negotiate a Guaranteed Maximum Price contract. Individual trades were solicited in a competitive bidding process and construction was substantially completed in Q4-2012. Site plans and a full life safety and code compliance report was produced for the Town of Bedford and reviewed by Town officials to obtain all necessary permits. Occupancy in the office areas was completed in December and 1366 vacated the premises of 45 Hartwell Ave the week of December 17th. Existing laboratory equipment and furnaces were moved that week and full occupancy of lab space at Preston Court was granted Jan 15th including a new chemical use permit. Direct Wafer furnace production re-commenced on Jan 21st and the majority of cell making operations re-commenced in February.

A Grand Opening celebration was held on January 31st, 2013 which included more than 300 invited guests. Below are photos of the new space including major equipment installed in the newly designed facility.



Figure 4: Office space and characterization room at 6 Preston Court.



Figure 5: Invited guests at the Jan 31st Grand Opening and Lab Tours



Figure 6: Production equipment installed at 6 Preston Court.

In general, the construction and move went smoothly and operations were able to resume without significant disruption. However, the Energy Recovery Unit that was delivered for installation did not meet the order specification. A temporary make up air unit was installed to meet the immediate needs of the building, which alleviated impact to lab operations. The final remedy was to order and install a second make up air system.



Figure 7: Energy Recovery Unit (left) from AnnexAir which did not meet specifications and temporary make up air system (right) installed to meet lab requirements.

As part of the transition to the larger facility, 1366 made an investment in a higher throughput SiN_x PECVD system. The new system increased batch size from 4 wafers to 50 wafers and provided some performance benefit as well. The new system was installed in May of 2013, and prior to the installation 1366 outsourced some fabrication of solar cells to institutes, particularly for SiN_x deposition.



Figure 8: PECVD SiN_x system (right) and gas cabinets and cooling water system (left).

Task 3: Build and Operate First Two Production Furnaces

The rapid nature of the Direct Wafer growth process developed using the Demonstration Furnace did not require significant changes to the growth itself to meet production throughput targets, but the furnace design and architecture underwent revision because of the sequence of operations before and after wafer growth. A variety of conceptual designs were reviewed to improve the takt time for wafer production from approximately 90 seconds on the Demonstration Furnace down to ~20 seconds, the target takt time to meet production cost goals.

A wafer trimming and quality control subsystem was also designed during this period to unload grown wafers from one of the furnace stations, trim the edges to 156mm square, and inspect wafers for quality metrics including geometry, surface defects, thickness and bow, followed by coin stacking of wafer output.

Detailed engineering design was completed with Purchase Orders placed for all major components by December 2012, meeting that milestone slightly ahead of schedule. The majority of parts were delivered within short lead times of < 8 weeks. However, a single, select vendor could not meet one component delivery date delayed the commissioning on the new furnaces by slightly over one month. First melting of silicon occurred at the end of March 2013.

The second major milestone in this task, providing 100 wafers at target thickness and efficiency, was submitted to DOE on April 30th. Because the wafer growth process is very similar to that of the Demonstration Furnace, the wafer bulk electrical quality was measured to be very similar. This was validated both by lifetime measurements on all of the 100 wafers, as well as cell processing done on some of the wafers.

An expedited cell lot was also made including wafers from both furnaces and the electrical quality was determined to be very similar and met the milestone requirements with a report from NREL on May 7, 2013.

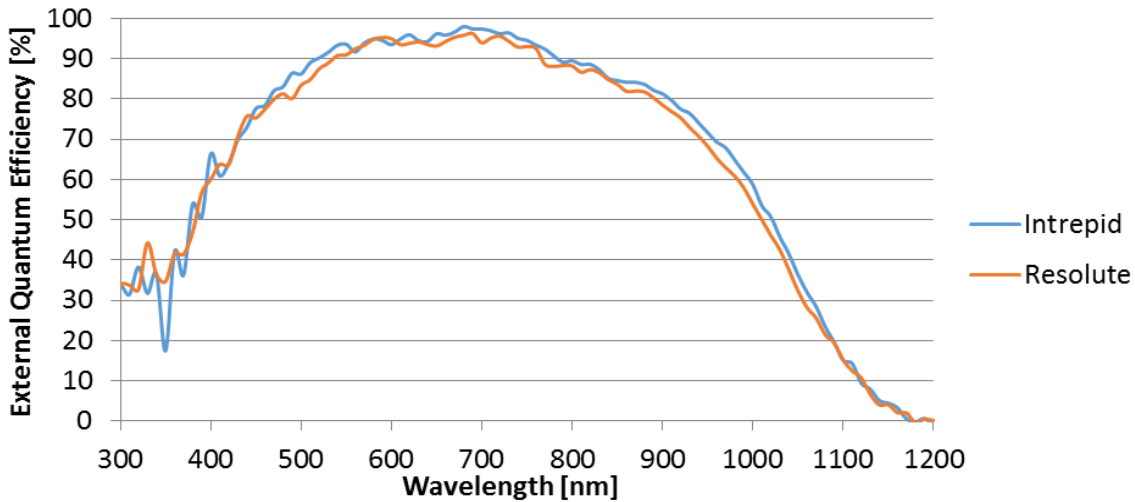


Figure 9: Comparison of EQE on untextured solar cells produced from Demonstration Furnace (Resolute) and new Production Furnace (Intrepid).

Following the initial startup of the furnaces, there continued to be subsystems that were upgraded and added additional functionality to the furnaces. One of these functions was the wafer unloading, laser trimming and inspection.

The wafer unloading system as originally designed was not sufficiently robust and resulted in failures to remove wafers of approximately 5%. This was not acceptable because it would require stopping grown and incurring significant lost time to manually remove wafers. A new design was implemented and installed in early August 2013, which was the primary enabler of increased throughput to meet the subsequent milestone of >1000 wafers/day. The new wafer unloading system proved to be very robust and the first attempt at 24 hours of production was successful at producing a yielded output of 1226 wafers. As shown below, the average resulting production rate was 51 wafers/hour.

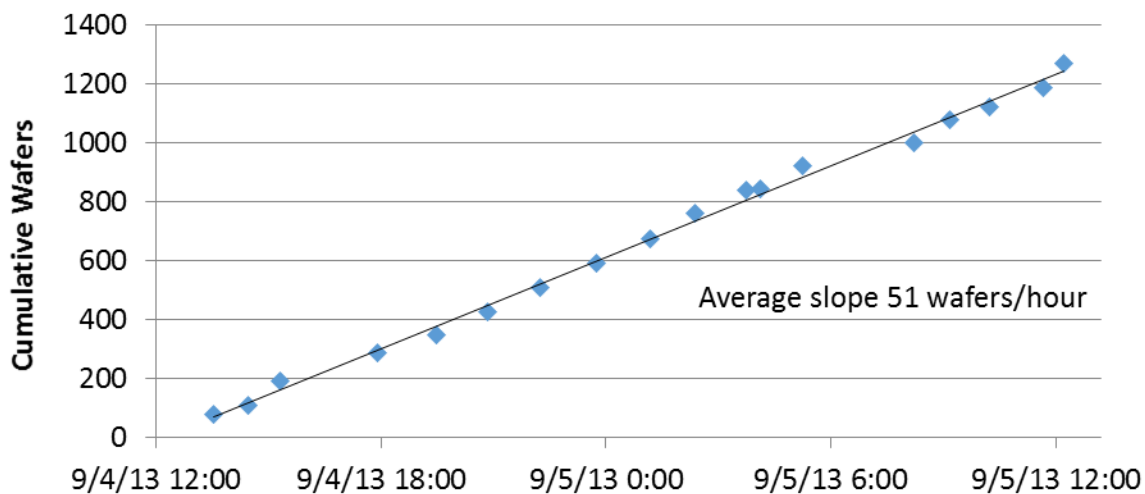


Figure 10: Production rate of Direct Wafers over a 24 hour period.

For validation of cell efficiency, wafers selected for processing into solar cells were sent to Korea for texturing with RIE by an equipment vendor, and then processed internally through our baseline process. The table below provides internal measurements of resulting cell performance.

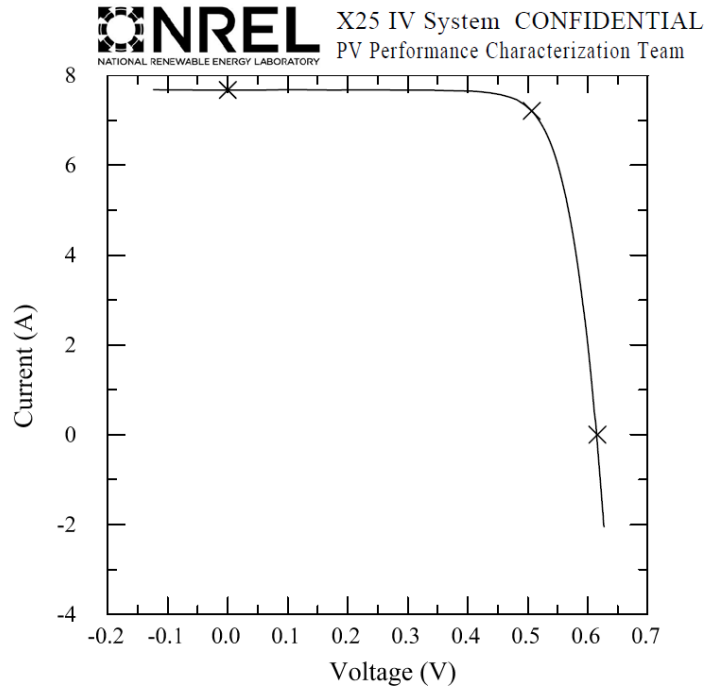
Wafer ID#	Voc [V]	Jsc [mA/cm ²]	FF [%]	Eff [%]
IN023-0052	0.614	34.9	78.3	16.81
IN023-0100	0.608	34.7	78.2	16.50
IN023-0163	0.612	35.2	78.2	16.83
IN023-0162	0.613	35.0	78.2	16.78
IN024-0040	0.609	35.2	78.1	16.74
IN024-0046	0.607	35.1	78.0	16.59
IN024-0051	0.611	35.4	78.2	16.89
IN024-0052	0.610	35.1	78.0	16.70
IN024-0056	0.613	35.4	78.2	16.94
IN024-0058	0.611	35.2	77.4	16.66
IN024-0059	0.612	35.3	78.4	16.94
IN024-0076	0.610	35.2	77.7	16.68
IN024-0097	0.613	35.2	78.4	16.93

Figure 11: NREL Measurement of solar cell produced from Production Furnace Intrepid.

The set of wafers were sent to NREL for testing, which resulted in slightly higher Voc measurements, but lower FF and Jsc. The measurements by NREL for one of the cells is shown in Figure 12.

1366 Technologies multi-Si Cell

Device ID: IN024-0056 Device Temperature: 24.8 ± 0.5 °C
Sep 12, 2013 08:58 Device Area: 226.1 cm^2
Spectrum: ASTM G173 global Irradiance: 1000.0 W/m^2



$V_{oc} = 0.6162 \text{ V}$	$I_{max} = 7.2066 \text{ A}$
$I_{sc} = 7.6767 \text{ A}$	$V_{max} = 0.5068 \text{ V}$
$J_{sc} = 33.960 \text{ mA/cm}^2$	$P_{max} = 3.6525 \text{ W}$
Fill Factor = 77.22 %	Efficiency = 16.16 %

Figure 12: NREL measurement of solar cell produced from Production Furnace Intrepid.

The basic design architecture selected for the Production Furnaces was validated during this period with the 2 initial furnaces and was able to accommodate minor re-design of some subsystems such as the wafer unloading.

Task 4: Business goals to support expansion to 40 MW/yr

1366 selected 5 leading cell manufacturers worldwide to provide sample Direct Wafer product for evaluation as part of developing strong business relationships. In spite of a challenging wafer oversupply in the market in 2012 and 2013, there remained significant interest in long-term cost reduction opportunities in wafers. Our wafers offered – and continue to offer – an excellent opportunity to improve profitability for cell manufacturers that are currently operating with very tight margins.

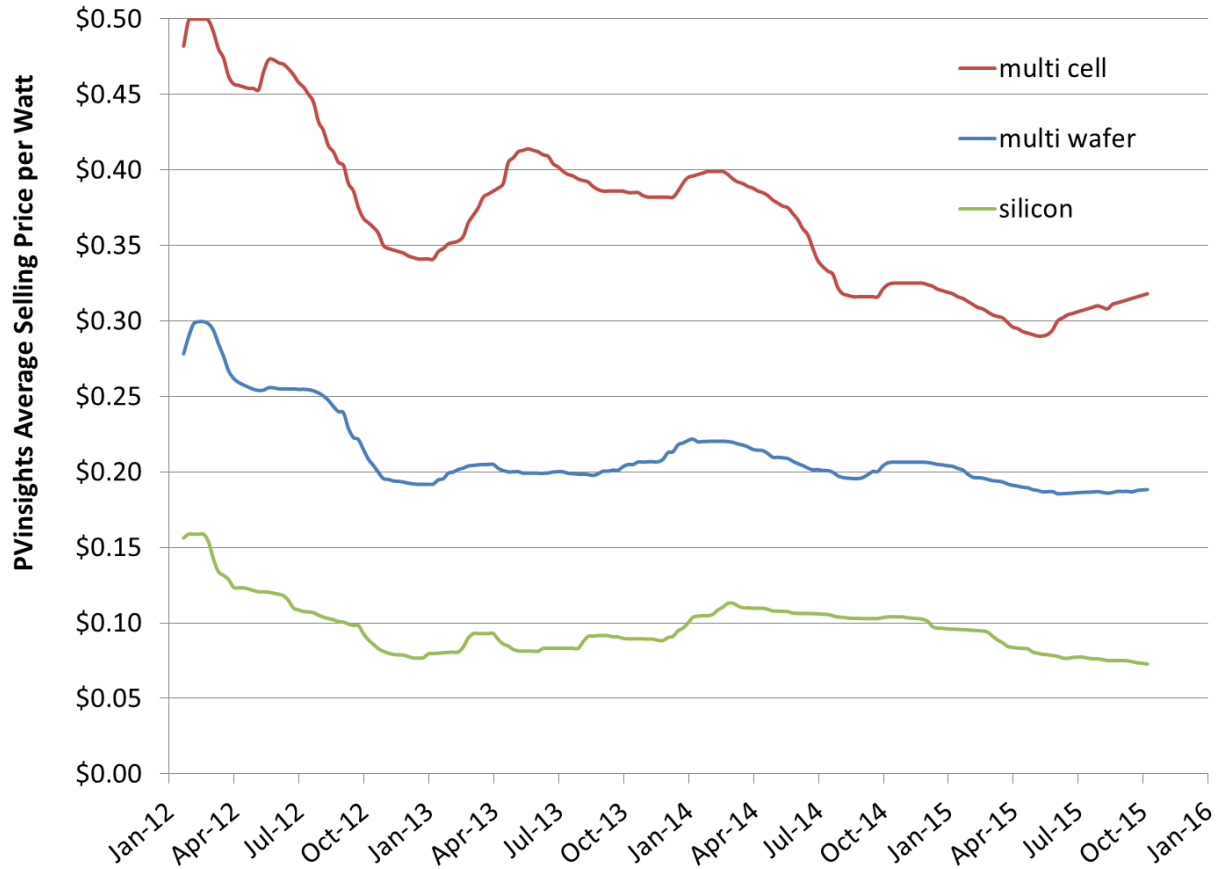


Figure 13: Market pricing history for multicrystalline silicon as tracked by PV Insights.

Early trials demonstrated >17% average efficiency and comparison by the manufacturers against their standard multi wafers were within 1.0% to 0.5% absolute efficiency.

The most significant difference between Direct Wafer products and standard sawn multicrystalline wafers is the surfaces and their texture. Because the as-grown surfaces of 1366's wafers do not respond to the industry standard iso-texture wet etching, a unique texture must be used and in most cases this is provided by 1366 to ease market adoption. The texturing solution selected by 1366 for implementation for our 40MW factory is Reactive Ion Etching, which was first applied commercially to solar cells nearly 10 years ago. 1366 leveraged this existing infrastructure for use with our products and selected a solution that delivered high levels of cell performance. We also considered tool cost of ownership, business financial stability and willingness to commit resources to collaborative development and tolling services prior to a delivery of a new RIE machine to 1366. A purchase order was placed in mid-September 2013 for an RIE system that was installed at 1366 in Q1-2014.

To coincide with 1366's shift in focus from R&D to production, several new business systems were also implemented during this period that encompassed design, purchasing, Environmental Health and Safety and production.

Task 5: Prepare for Additional Capacity

As 1366 readied for additional capacity, the company made a number of facility and staffing upgrades to assist with demonstrating 24/7 production of 3 new Direct Wafer furnaces along with supporting upstream and downstream processes.

To accommodate anticipated increases in throughput, 1366 undertook two initiatives associated with the facility and its equipment. The first was an expansion and upgrade of the demonstration factory to accommodate scale-up and the second specific to the selection of new equipment to assist in meeting production targets. The installation of a qualified 5-lane production wet bench for customer product was completed and the system was commissioned having undergone an extensive hazard review to ensure proper facilities support and safety policy implementation.



Figure 14: Empty Space for Expansion after Demolition as First Part of Phase 1b Construction.

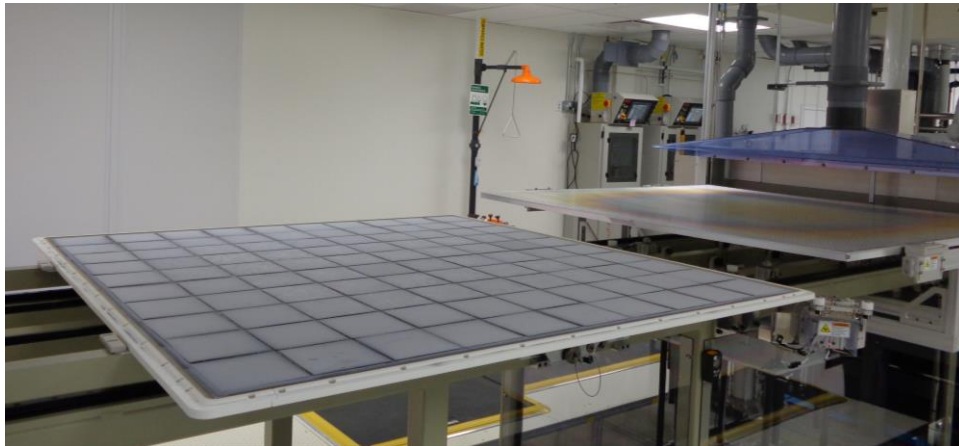


Figure 15: Tray of 100 wafers loading into RIE process for texture. Equipment installed in part of space shown in Figure 14.

Staffing was also adjusted to ready for the production surge and the company trained a crew of operators to run the Direct Wafer furnaces, moving the sole responsibility away from the engineering team. The new hires resulted in increased productivity as shown below.

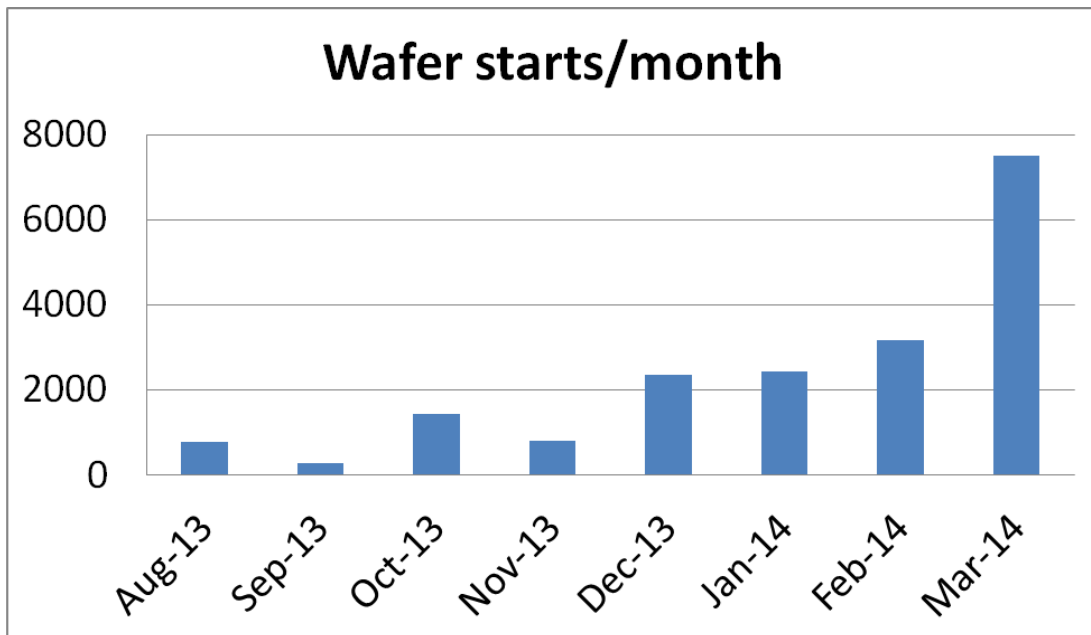


Figure 16: Wafer Production from Gen2 Production Furnace Intrepid

With the tools and staffing in place, higher volumes of Direct Wafer products became available for customers and a 1000 wafer shipment was produced for a leading customer. These wafers were used for cell processing and subsequent fabrication into initial modules corresponding to Milestone 5.1 (the manufacture of five 60 cell modules > 223W each). These first modules were rated 240-245 W. 1366 conducted numerous

trials at different customer production lines and demonstrated cell efficiency averaging 16.9% without any process changes, well above the 5.2 Milestone goal of >16.0%



**Figure 17:
Preparation of
1000 Direct
Wafer
Products for
Customer
Shipment**

One benefit of the installation of two initial production furnaces, was the ability to improve hardware on one machine while using the other to implement process improvements and provide product to customers. This allowed us to make several design improvements and test them out on the first set of production furnaces prior to engaging in the subsequent build-out.

Task 6: Furnace Build-Out

As the company aimed to complete the build of three Generation 3 Production Direct Wafer furnaces, its team made a series of design improvements to achieve increased throughput, higher duty cycle, significant capex reduction and improved wafer quality. The production furnaces will provide the platform for the Company's subsequent GW expansion. The first Gen3 production furnace was commissioned in January 2015 and the 2nd and 3rd furnaces were installed within 60 days following.

Wafer production for customers continued to be supplied from the initial 2 production furnaces during the ramp period for the furnaces. The first 20 modules of the 10kW field installations for Milestone 6.2 were fabricated at two different manufacturers in Asia and delivered to IHI Corporation, a major infrastructure company in Japan with \$10B annual revenue. IHI is also the largest land owner in Japan and is expanding into PV installations. The first Global Direct Wafer Module Test Site was constructed for IHI in Sakura City, Tochigi, Japan. A ribbon cutting ceremony was held with two representatives from 1366 present for the live connection of the modules to the grid and monitoring system.



Figure 18: IHI Ceremony and Commissioning of 20 Direct Wafer Modules in Tochigi, Japan

During Q2, 1366 began to ship commercial product from the new Gen3 furnaces and an additional 25 Direct Wafer modules were produced by a manufacturer in Europe, with 10 of the modules added to the IHI test site in Japan and the additional modules installed at a tier one cell manufacturers test site in Germany (image below) for completion of Milestone 6.1.



Figure 19: Installation of Direct Wafer Modules for Field Monitoring in Germany

With the production furnaces in place and running, customer shipment sizes increase to 1000 wafer batches sizes which also enabled a variety of cell process variations to be

explored. While many of these adjustments are confidential to the cell manufacturer and cannot be disclosed, 1366 demonstrated lot averages of 17.4% efficiency on a production line without any adjustments or process changes, completing milestone task 6.2.

Task 7: Operations and Evaluation of Full Set of Production Furnaces

With three Gen3 Production Furnaces installed, 1366 optimized operations for both product quality and production costs and demonstrated the economic viability of the furnaces when running at high throughput.

With the successful furnace ramp-up, 1366 began shipping product from these new furnaces to customers and achieved record levels, including a lot average of 18.3% meeting one key requirement of Final Deliverable 2 and exceeding the >16.0% requisite milestone at high volume. Figure 20 clearly demonstrates the strong consistency between two 1366 production furnaces.

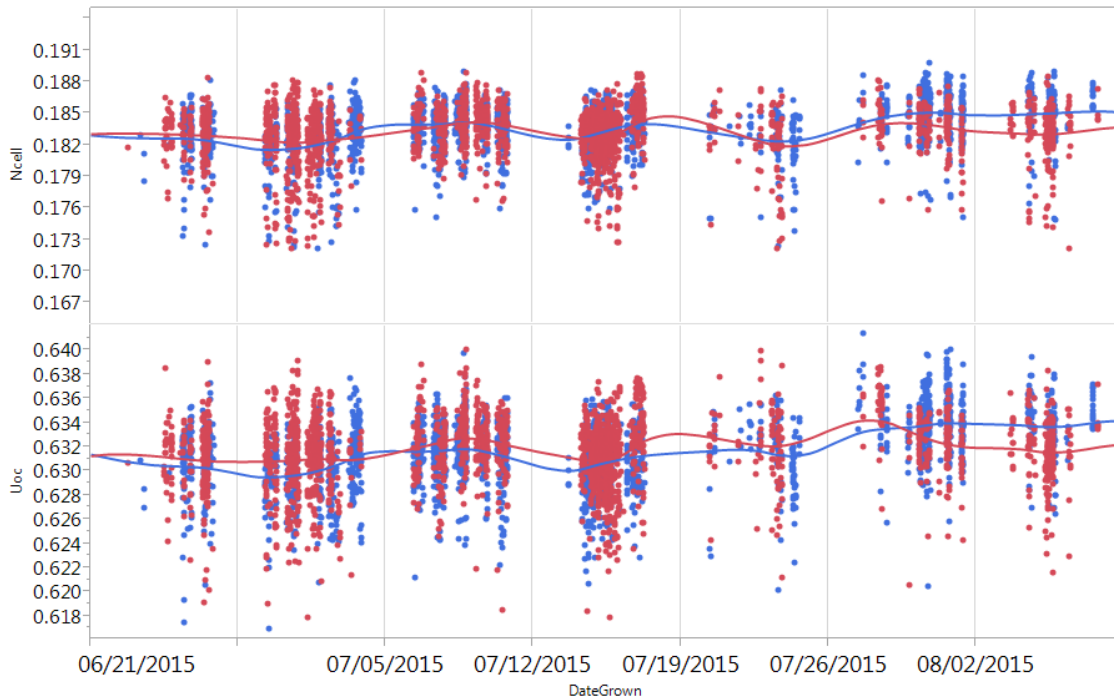


Figure 20: Average 18.3% efficiency for 10,000+ Cells. Blue and red correspond to source Gen3 Production Furnaces 3 and 4.

Having demonstrated greater efficiency potential with the new furnaces, the equipment team continued to make hardware improvements to advance operating metrics. The operating time on the furnaces continued to increase, making the furnaces ready for their first production campaign. 1366 operated the campaign and collected direct operating metrics from the furnaces to demonstrate adjusted COGS <\$.19/W as shown in Figure 21, confirming the economic viability of the Direct Wafer process at scale and meeting the second key requirement of Final Deliverable 2.

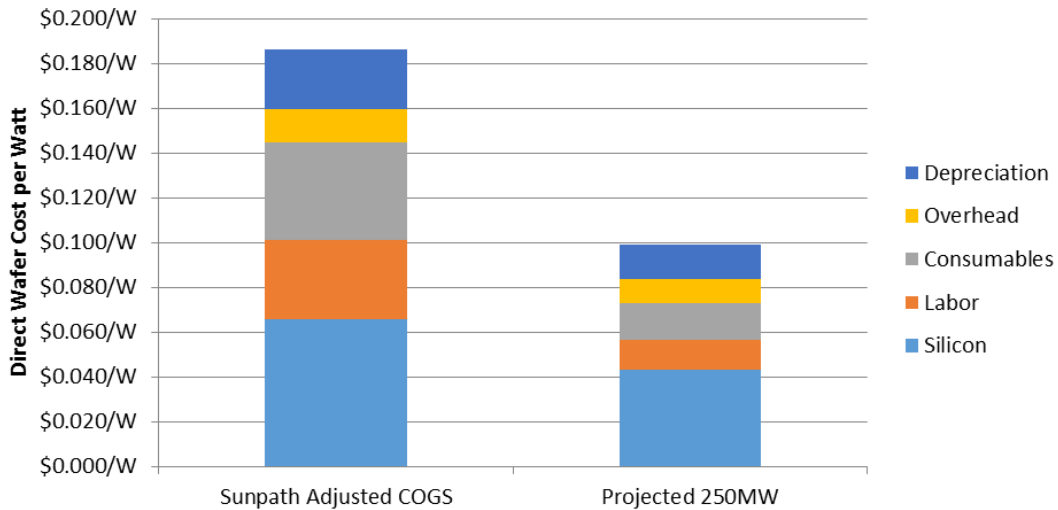


Figure 21: Confirming the Economic Viability of the Direct Wafer Process at Scale

1366 partnered with General Electric, which has a PV test site at its energy headquarters in Schenectady, New York, for the first field installation in the United States. The site (shown below) accommodated an array of 192 panels in a utility-style mounting system that is configured with max power point trackers for each pair of modules. The 50 kW site provides meaningful data collection as well as comparison between Direct Wafer modules and reference modules. It also satisfies Final Deliverable 1.



Figure 22: 50kW Installation of Direct Wafer modules at General Electric in Schenectady, NY

1366 signed a strategic partnership with Hanwha Q Cells, a relationship furthered by earlier successful trials. The partnership also fulfilled the sales contract requisite for 40 MW of Direct Wafer products. Details of the achievements made between the two companies can be found in this press release: <http://bit.ly/1Qi3G6P>. A key achievement of the partnership was the demonstration of cell efficiency >19% with Direct Wafer

product fabricated into cells on their industrial line. Cell results were certified by Fraunhofer CalLab as shown in Figure 23.

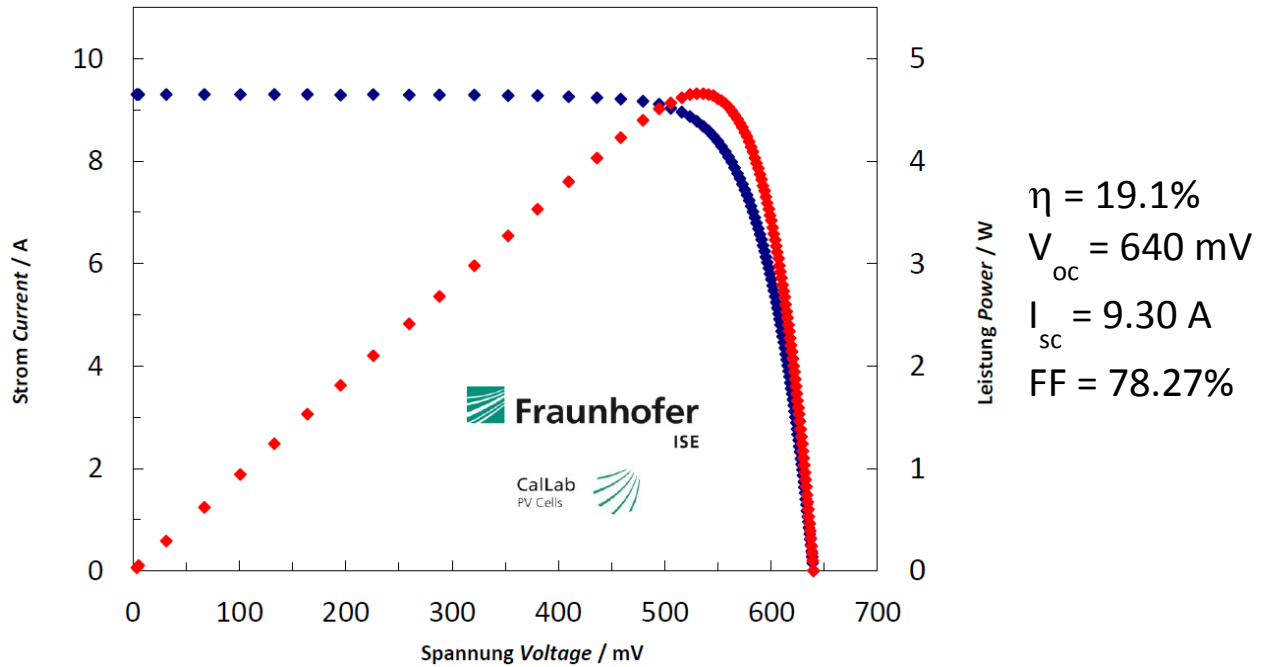
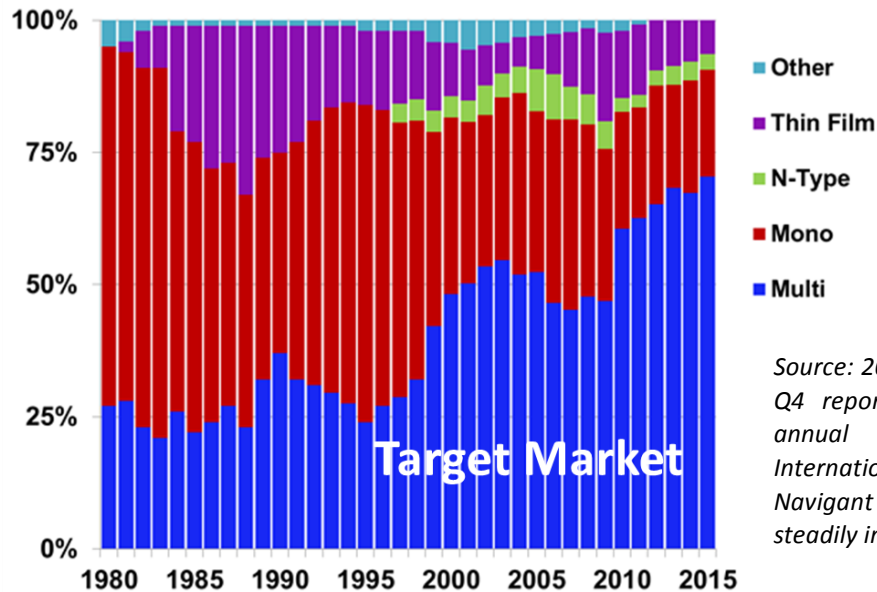


Figure 23: Certified cell efficiency achieved on industrial line at Hanwha Q Cells

COMPETITIVENESS IN THE MARKETPLACE

Our disruptive technology addresses an \$8 billion market at 50% of the cost, 60% of the capital, and 30% of the energy use compared to conventional casting and sawing manufacturing. Some prevailing opinions from industry observers state that the market is moving towards advanced thin film structures and high efficiency mono-crystalline wafers. Although it is difficult to predict the future, looking at historical trends – that includes data from both the start and end of the award period – suggest this forecast may not hold true. In fact, multi-crystalline continues to gain market share as seen below. Multi has steadily increased market share against competing monocrystalline (higher efficiency but also higher cost) and thin film (cadmium telluride and CIGS) technologies over the last thirty years due to a superior efficiency versus cost profile. Multi-crystalline technology continues to deliver the lowest LCOE in the market.



Source: 2010 - 2015 Data from IHS 2015 Q4 report; 1999 - 2009 Data from annual March issue of Photon International; 1980 - 1998 From 2008 Navigant Consulting report. Multi has steadily increased market share.

Figure 24 – Historical PV market share by technology

The multi segment is 1366’s target market. The total installed capacity for conventional crystalline silicon in 2016 is estimated by IHS to be 67 GW_p. The strength of the Direct Wafer technology is its compatibility with this installed base.

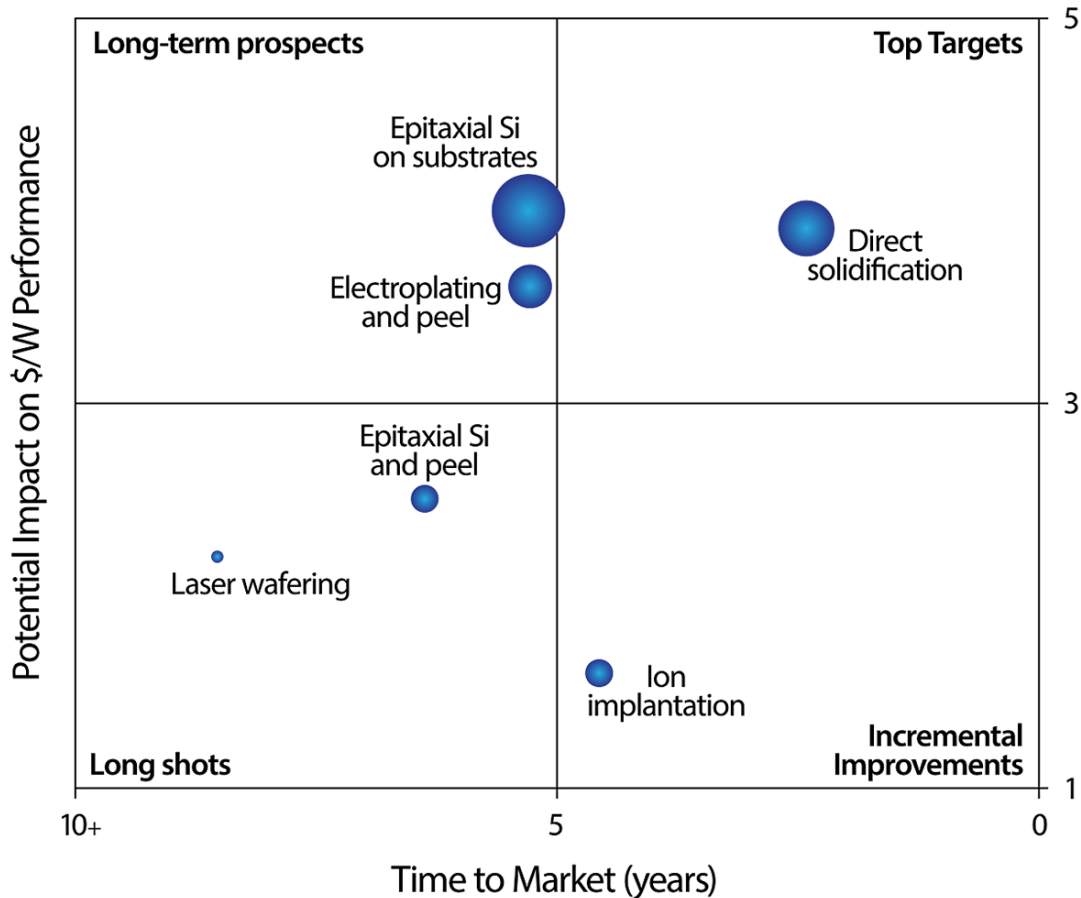
As 1366’s technology will further strengthen these trends with a disruptive solution that allows downstream customers to both realize 5% to 10% improvements in their margins and build a long-term, differentiated product roadmap that leverages their existing billion dollar cell and module investments built around the industry standard 156 mm wafer.

Competitive Technologies

There are several different methods for producing “kerfless” silicon wafers without casting and sawing: solidifying melt either against a substrate (includes Direct Wafer) or as a vertical ribbon, ion implantation and cleaving, exfoliation, and epitaxial growth. Growth of vertical ribbon was commercialized but unable to stay competitive due to a combination of very low throughput, non-standard geometry, and high dislocations resulting from curvature in thermal gradients. Other technologies are in development, and all have their own challenges and opportunities.

An independent study of “Game Changers in PV” published by Lux Research summarized the market opportunity and time to market for competitive wafer technologies, as shown in Figure below. The Direct Solidification approach, such as Direct Wafer, is identified as a top target because of the potential value impact as well as short time to market as it delivers “standard” 156mm, 200µm-thick wafers that can “drop-in” to the existing cell and module supply chain and therefore can be adopted

rapidly. The other alternative technologies produce ultrathin wafers (<50µm) with silicon usage < 1 g/W.



Source: Lux Research

Figure 25 – Potential Impact and Time to Market of Competitive Kerfless Technologies

Competitive Analysis

For decades, companies and institutes have tried with limited success to produce “kerfless” wafers by Direct Solidification due to the inherent advantages of high throughput and low cost. 1366 Technologies is the first company to solve the challenge.


The ultra-thin kerfless wafer technologies that produce 20µm to 50µm-thick wafers (ion implantation and cleaving, epitaxial growth, and metal bonding and exfoliation) have the potential for high efficiency modules and <\$1/W installed system costs but face serious adoption and technical challenges. Thin wafers can be both a feature and a limitation, since it lowers silicon cost, but forces the companies to find simultaneous solutions to several challenges imposed by ultra-thin wafers, such as downstream cell and module handling without breakage, rear surface passivation, and integration into cell and module production lines. Each of these companies must address all of these challenges



at once to deliver a high efficiency module product and then validate its bankability. All problems must be solved for the technology to gain rapid adoption in the market. If successful, it would displace or transform the majority of the current silicon PV supply chain. In contrast, 1366 Direct Wafer aims to leverage the existing infrastructure and astounding progress in cost reduction over the past few years – and during the tenure of this award – made by silicon PV companies throughout the value chain.

Multi-Si wafers are a commodity product with standardized size, purity, and electrical specifications. Although there is some variation in wafer electrical quality, the majority of wafer manufacturers produce similar classes of products. Wafer manufacturers compete on their ability to optimize the standard wafer process to increase efficiency and lower cost, gain economies of scale, and exploit geographic cost advantages (labor, electricity, etc.). There is minimal technology differentiation as most wafer suppliers utilize similar processing equipment purchased from the same equipment suppliers. The relatively high concentration of wafer competitors (top 10 competitors >70% of the market) is a function of the capital costs required to enter the market and the state support that many companies, particularly in China, have received to achieve scale. Given that economies of scale play a big role in manufacturing cost, it is highly likely that over time, there will be consolidation in the market and the level of concentration will be even higher in the future.

Nearly all of the top wafer manufacturers will compete with 1366’s Direct Wafer technology based on the standard ingot casting and wafering technology as described in earlier sections. There is very little differentiation between product offerings for each of the major pieces of equipment (casting, cutting, cropping, and sawing) as listed in Figure 26 below. The standard wafer equipment requires a capital investment of \$0.15/W (without recycling or building costs) and delivers an average wafer production cost of ~\$0.21/W. The standard technology wastes 50% of the silicon in the cutting and sawing process and has high consumables cost due to the one-time use of crucibles in the casting process and the steel wire in the sawing processes.

Figure 26 – Competitor Equipment

Process Step	Suppliers	Ave. Throughput	Ave. Throughput	Ave. Capex (\$/W)
Ingot Casting	Jinggong (China) ALD (Germany) Cyberstar (France) GTAT (US/China)		16MW/yr	\$0.05/W

Brick Cutting	Dalian Linton (China) Jinding (China) Abwood (UK) Applied Materials (US) Logomatic (Germany)		200MW/yr	<\$0.01/W
Cropping	Abwood (UK) H-Arnold (Germany)		140MW/yr	<\$0.01/W
Sawing	Dalian Linton (China) Meyer Burger (Germany) Applied Materials (US) Komatsu (Japan) Logomatic (Germany)		9MW/yr	\$0.09/W
TOTAL				\$0.15/W

The wafer equipment market used to be dominated by German and US suppliers, such as GT Solar and Meyer Burger, but is increasingly controlled by Chinese vendors. This is especially true for casting technology which is fairly simple and can be copied by lower-cost Chinese vendors. For more complicated process, such as sawing, which depends on high yields and reliability to deliver lower costs, the European vendors have managed to maintain solid market share. But the Chinese vendors are increasingly attacking these markets.

1366 intends to win on all key product dimensions with its Direct Wafer technology by delivering a simple, scalable process that produces standard 156mm size wafers at 50% of the cost, 60% of the capital, and 30% of the electricity of conventional casting and sawing processes. The Direct Wafer process also offers customer CTO's technology roadmap upside as it can deliver more uniform quality wafers that have special features.

DELIVERABLE / MILESTONE DEVIATIONS

Decreases in silicon, wafer and cell pricing led to adjustments in milestones and deliverables associated with the project. At the conclusion of Budget Period 1, a SOPO modification was made to reflect the changing market conditions of lower selling prices and higher efficiency. Specifics are outlined below.

Task 4.1

- For market introduction of Direct Wafer product, there was a limited number of cell manufacturers with capabilities for texturing kerfless wafers. It was necessary for 1366 to invest in production scale texturing equipment, which was added to the scope of Task 4 and the installation of RIE texturing equipment at 1366 was added as Milestone 4.1

Task 5.0

- Milestone 5.1 was changed from delivery to DOE of 1kW modules with >15% efficiency to require the module fabrication be conducted by an external manufacturer with >100MW/yr capacity and a target power of >223W (15.5% at 98% CTM). This provided better validation of customer acceptance in the marketplace.
- Milestone 5.2 similarly increased target efficiency to 16.0% from 15.5%. These efficiency adjustments were made to reflect changing market conditions and efficiency gains from conventional methods, particularly the improvements to DSS casting processes to incorporating seeding and production of High Performance Multi (HPM) sawn wafers.

Task 6.0

- Milestone 6.2 similarly increase efficiency for the first 1000+ wafers grown from the Gen3 production furnaces from an initial target of only 15%, to 16.5%.
- Milestone 6 including the installation of 10kW and was changed to no longer include the DOE Regional Test Center (RTC) baseline procedure and rely on the module manufacturer data instead in connection with subsequent field monitoring.

Task 7.0

- Final Deliverable 1: The milestone original requirement of a 60 kW module at >15% efficiency installation at a customer site with RTC baseline procedure was adjusted to 50 kW install at >16% efficiency based on the selection of an existing site that only had physical space for 192 modules (60 cells each). 1366 met this goal with a new installation of modules featuring Direct Wafer products at the General Electric energy headquarters in Schenectady, New York.
- Final Deliverable 2: 1366 increased the original adjusted COGS Test of <\$0.25/W and >16% efficiency based on a high volume test >40kW. The final target was set to <\$0.20/W and >16.5% efficiency. Achieving values were an adjusted COGS of \$0.19/W and averaging 18.3% efficiency.

SUBJECT INVENTIONS, PUBLICATIONS, AND PRESS RELEASES

Publications/Presentations

- “Direct Wafer – High Performance 156mm Silicon Wafers at Half the Cost of Sawn” at the Crystalline Silicon oral session of EUPVSEC 2013

Press Releases

- 1366 Technologies Achieves New Technical Milestones, <http://bit.ly/1OcHgCO>
- IHI to Deploy 1366 Technologies Direct Wafer Products, <http://bit.ly/1XtTL40>
- 1366 Technologies Recognized as Bloomberg New Energy Pioneer, <http://reut.rs/1QExQ4I>
- 1366 Technologies and Hanwha Q CELLS Form Strategic Partnership, <http://bit.ly/1EjoiBs>

Media Articles

- *PV-tech*, Hanwha Q Cells Confirms 19.1% Cell Efficiencies with 1366s Direct Wafer Technology: http://www.pv-tech.org/news/hanwha_q_cells_confirms_19.1_cell_efficiencies_with_1366s_direct_wafer_tech
- *PV-tech*, 1366 Meets 5 MW Furnace Milestone: http://www.pv-tech.org/news/1366_technologies_meets_5mw_per_furnace_milestone
- *PV-tech*, China and Japan Get Interested in 1366 Technologies: http://www.pv-tech.org/news/china_and_japan_get_interested_in_1366_technologies_direct_wafer_technology
- *The Boston Globe*, 1366 Opens New Wafer Manufacturing Plant: <http://www.boston.com/businessupdates/2013/01/30/lexington-technologies-opens-solar-wafer-plant/WkKeGBCg5lxCBwqfC5RFJK/story.html>
- *CleanTechnica*, Solar as Cheap as Coal, Why Not Cheaper: <http://cleantechnica.com/2015/03/06/solar-cheap-coal-not-cheaper/>
- *Greentech Media*, 1366 to Build 250 MW Factory in Upstate New York, <http://www.greentechmedia.com/articles/read/1366-Technologies-to-Build-250MW-Direct-Silicon-Wafer-Factory-in-Upstate>