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- Presentation Title: Medium Voltage DC Solid-State Circuit Breaker Based on a Cascaded Switch Topology
- Author(s): Luciano Garcia Rodriguez
- Organization(s): Sandia National Laboratories, and Mitsubishi Electric Power Products (MEPPI)

U.S. DEPARTMENT OF ENERGY | Office of ELECTRICITY

H1. 3.2 - Medium Voltage DC Solid-State Circuit Breaker Based on a Cascaded Switch Topology

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Project Overview

Project Description: Develop a medium-voltage DC (MVDC) solid-state circuit breaker (SSCB) featuring a ***cascaded switch*** topology. Each SSCB module is designed to allow for ***series and parallel connections of multiple modules***, enabling operations at higher voltages and greater power levels.

Period of Performance: 10/01/2025 – 09/30/2028 (3 years).

Award Amount: $1,200,000.

Prime Awardee: Sandia National Laboratories.

Partners: Mitsubishi Electric Power Products (MEPPI).

Technology Area: DC circuit breakers; Advanced power electronics.

Alignment with DOE and administration goals:

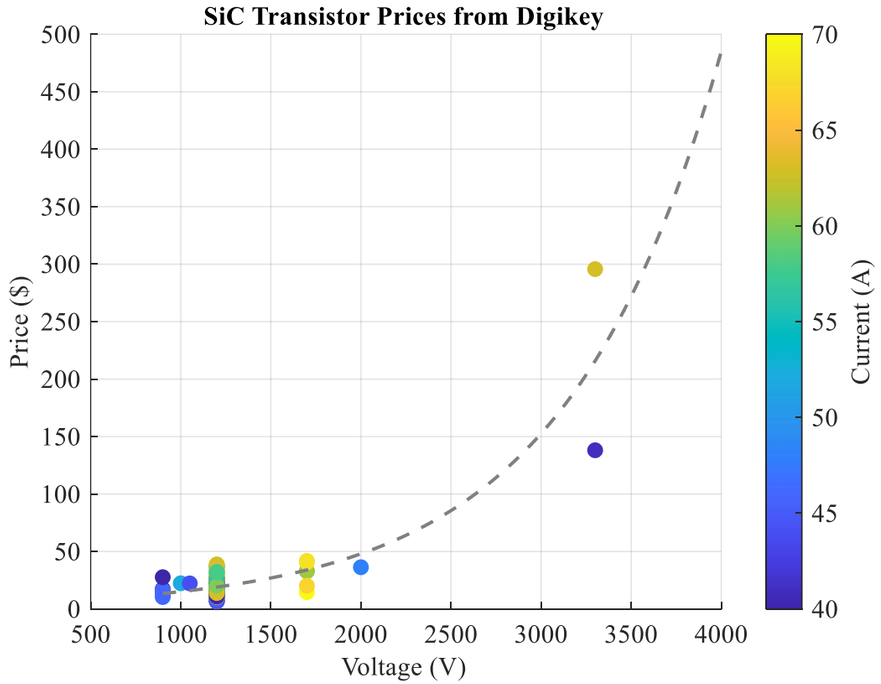
The DC solid-state circuit breaker project directly supports DOE Office of Electricity goals by enabling faster, more selective protection for emerging DC and hybrid AC/DC grid architectures.

By rapidly isolating faults, the technology helps **stabilize** the grid under reliability stress, **optimize** system performance through improved controllability and resilience, and **grow** future grid capacity by supporting HVDC transmission, renewable integration, energy storage, high-demand data centers, and other advanced power-electronics-based infrastructure.

Project Details: Problem Statement

- MVDC power distribution systems require fast, resettable and selective protection to isolate faulted sections while maintaining service to the rest of the network.
- DC fault protection is challenging because DC systems lack natural current zero crossings, making interruption more difficult than in AC systems. Fault currents can also rise rapidly and exceed the withstand capability of power-electronics-based converters.
- SSCBs offer sub-millisecond response, resettable operation, and improved protection coordination compared with mechanical breakers, but practical deployment is limited by cost, conduction losses, and the availability of high-voltage, high-current semiconductor devices.

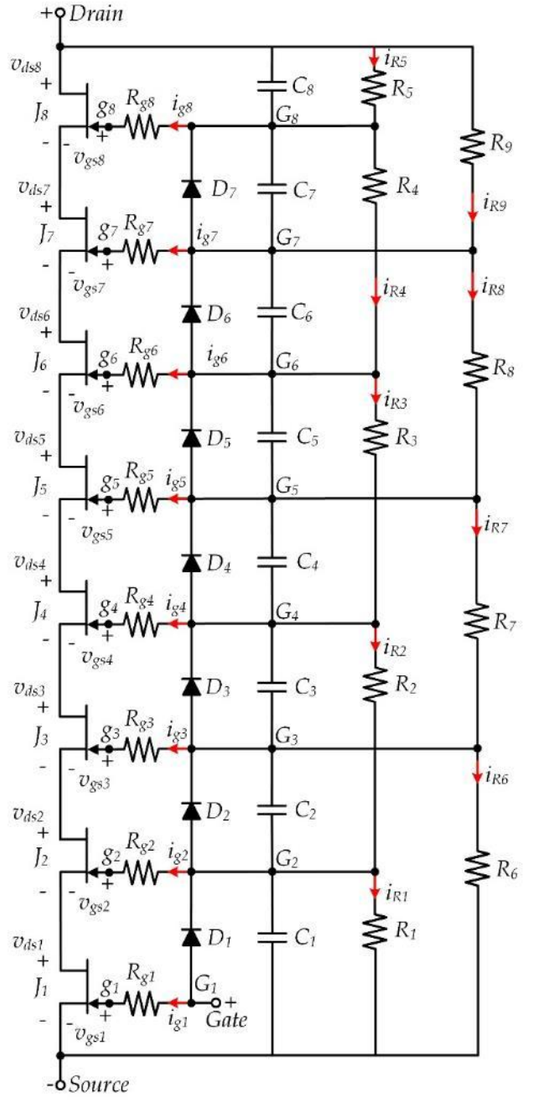
The lack of affordable, scalable, and readily available high-voltage semiconductor devices remains a key barrier to deploying SSCBs in MVDC systems for future grid applications, including renewable integration, energy storage, and high-demand data centers.



Project Details: Technical Approach / Innovations

- Developed a high-voltage, high-speed solid-state switch using a cascaded stack of lower-voltage, commercially available 1.2kV SiC JFETs and MOSFETs.
- The cascaded architecture enables high-voltage blocking capability while avoiding the cost and procurement challenges associated with single high-voltage semiconductor devices.
- A single low-side gate driver controls the full switch stack, reducing gate-drive complexity, isolation requirements, and system cost.
- By implementing either a MOSFET or JFET as the bottom device in the cascaded stack, the overall high-voltage switch can be configured to emulate an equivalent normally-off or normally-on HV device.
- Resistor and capacitor networks provide static and dynamic voltage balancing across the cascaded devices.
- Avalanche diodes provide overvoltage protection during switching transients.

This approach delivers a scalable, high-voltage, fast-switching platform at a fraction of the cost of comparable high-voltage semiconductor solutions.

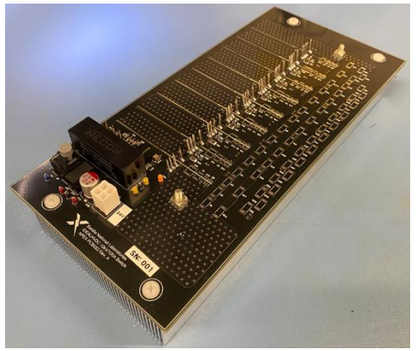


L. A. Garcia Rodriguez, L. Gill, J. Mueller, J. Neely, G. Baker, J. Flicker, E. Schrock, G. Pickrell, and R. Kaplar, "Cascaded SiC JFET Topology for High-Voltage Solid-State Circuit Breaker Applications," *in IEEE Transactions on Industry Applications*, vol. 59, no. 2, pp. 2326-2339, March-April 2023, doi: 10.1109/TIA.2022.3229655.

Project Objectives

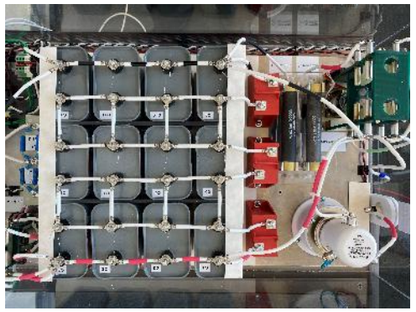
Budget Period 1: Single-Module MVDC SSCB Design and Demonstration

- ❑ Design a modular MVDC SSCB rated for 10kV/100A using a high-voltage switch topology based on lower-voltage, commercially available semiconductor devices.
- ❑ Build and experimentally validate a single SSCB module at 6kV/100A.
- ❑ Demonstrate fast switching performance with rise and fall transition times below 10µs.



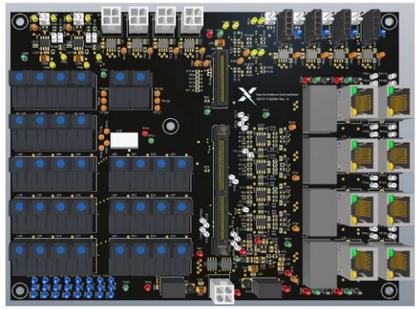
Budget Period 2: Two-Module Series and Parallel Operation

- ❑ Design and fabricate a high-insulation, high step-down-ratio DC-DC converter to power control boards, sensors, and gate drivers directly from the upstream MVDC bus.
- ❑ Implement and test two SSCB modules in series and parallel configurations.
- ❑ Demonstrate scalable modular operation up to 12kV.

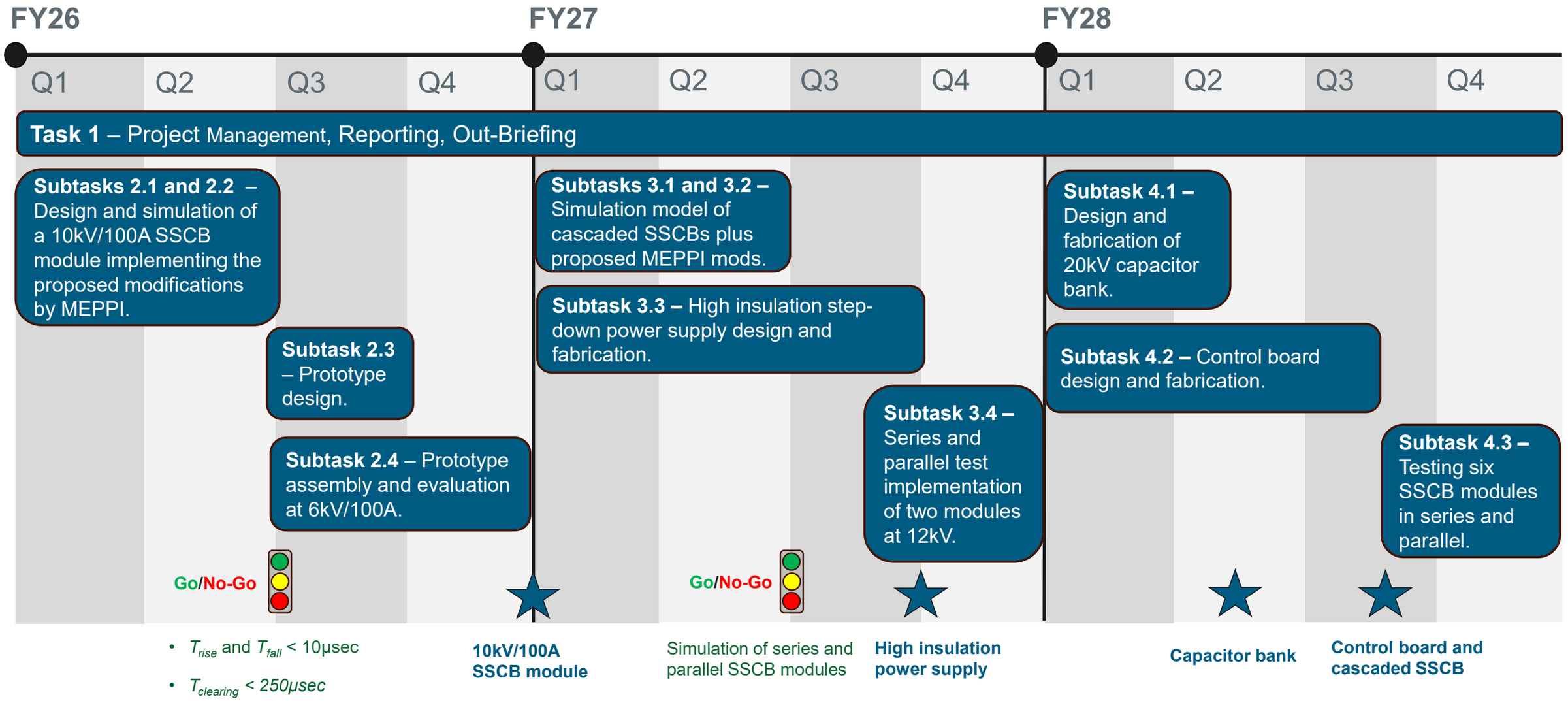


Budget Period 3: Multi-Module SSCB Demonstration up to 20kV

- ❑ Design and fabricate a 20kV capacitor bank to support extended high-voltage system operation and testing.
- ❑ Design and fabricate a centralized or coordinated control board capable of operating up to six SSCB modules.
- ❑ Test a multi-module series/parallel SSCB system and demonstrate operation up to 20 kV.



Timeline


FY26
FY27
FY28
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Task 1 – Project Management, Reporting, Out-Briefing
Subtasks 2.1 and 2.2 – Design and simulation of a 10kV/100A SSCB module implementing the proposed modifications by MEPPI.
Subtask 2.3 – Prototype design.
Subtask 2.4 – Prototype assembly and evaluation at 6kV/100A.
Go/No-Go
Subtasks 3.1 and 3.2 – Simulation model of cascaded SSCBs plus proposed MEPPI mods.
Subtask 3.3 – High insulation step-down power supply design and fabrication.
Go/No-Go
Subtask 3.4 – Series and parallel test implementation of two modules at 12kV.
Subtask 4.1 – Design and fabrication of 20kV capacitor bank.
Subtask 4.2 – Control board design and fabrication.
Subtask 4.3 – Testing six SSCB modules in series and parallel.
• T_{rise} and T_{fall} < 10µsec
• $T_{clearing}$ < 250µsec
10kV/100A SSCB module
Simulation of series and parallel SSCB modules
High insulation power supply
Capacitor bank
Control board and cascaded SSCB

Project Overview: Impact

DC System Protection Cost Reduction:

- Employing a cascaded HV switch configuration that utilizes ***lower voltage devices***, which are significantly less expensive than comparable high-voltage semiconductor devices, enables ***substantial cost savings.***

Scalable Protection in Higher Voltage and Power Applications:

- Once an SSCB module is optimized for a specific series configuration of devices, it can be ***cascaded for high voltage and power applications***, further reducing system costs.

Universal and Simpler Design:

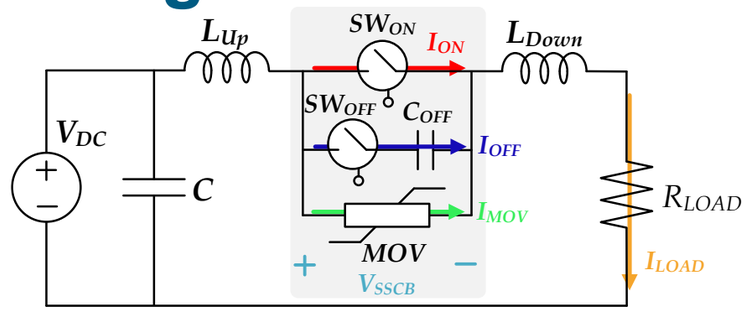
- The proposed SSCB topology reduces the necessity for extensive tuning of resonant components, frequently required to counteract parasitic elements in DC lines, reducing development time and costs related to prototyping and testing. Consequently, this approach can accelerate time-to-market and diminish overall project expenses.

The proposed SSCB approach has the potential to accelerate the adoption of medium voltage DC systems by eliminating the most significant barrier to their deployment.

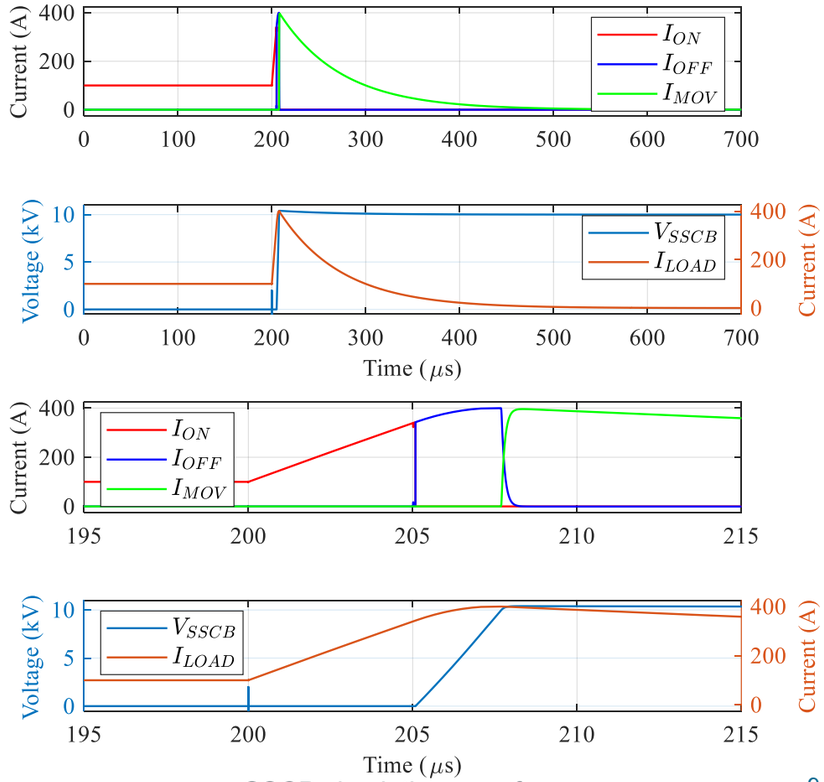
Proposed SSCB Operation and Transient Energy Management

- **Normally-on branch: i**mplemented using only SiC JFETs (ARPA-E BREAKERS).
- **Normally-off branch**: utilizes a combination of SiC MOSFETs and JFETs, with ongoing studies on a fully SiC MOSFET topology.
- **Shunt capacitor sizing:** Capacitor sizing balances voltage overshoot reduction against increased current stress, while the MOV clamps voltage and absorbs stored line energy.
- Upon fault detection, the normally-on branch opens and the normally-off commutation branch turns on.
- MVDC line cables modeled using upstream/downstream line inductances; L≈0.18 μH/m for short cable runs.

The capacitor should be the smallest practical value, that limits voltage overshoot and *dV/dt* under worst-case conditions so the SSCB devices remain within their safe operating area and the MOV can clamp the transient without exceeding its current, energy, or thermal ratings.

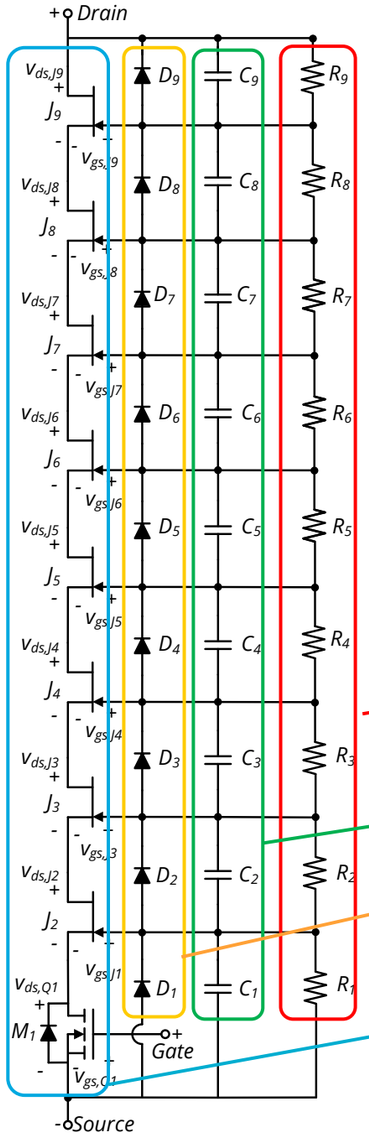


Proposed SSCB architecture in an MVDC system.



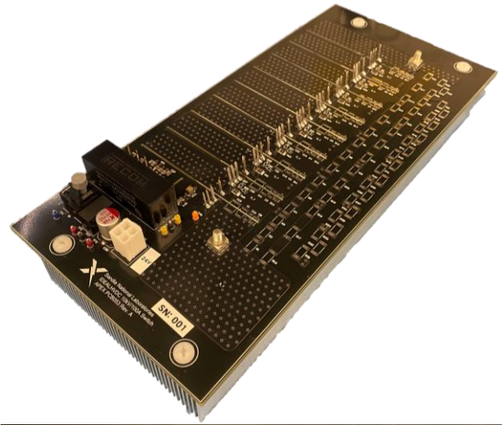
SSCB simulation waveforms.

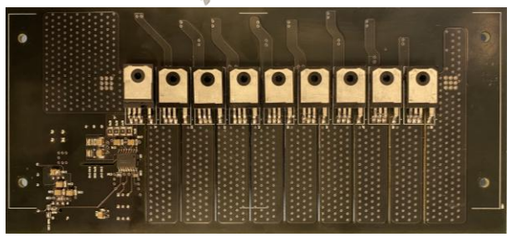
10kV/100A Normally-Off Cascaded Switch



Qtys	Device Specifications	Manufacturer/Part Number
Power Stage		
1	1.2kV/142A SiC MOSFET	Infineon / AIMZH120R010M1TXKSA1
8	1.2kV/120A @ T_c = 112°C SiC JFET	Onsemi / UF3N120007K4
Gate Driver Circuit		
1	Dual Channel IC Gate Driver	Texas Instruments / UCC21551CQDWKRQ1
1	DC/DC Converter 24V/3W	Recom Power / RHV3-2424S/R20
Circuit Protection		
8	Diode Avalanche 1kV/1.5A	Vishay BYG23M-E3/TR3
8	Schottky Diode 60V/1A	Vishay VS-10MQ060NTRPBF
8	24V/0.5W Zener Diode	SMAZ5934B-E3/61

- ❑ Static Balancing Network (single and dual networks were implemented).
- ❑ Dynamic Balancing Network.
- ❑ Transient Overvoltage Protection Components (gate-source protection devices not shown).
- ❑ Active Devices.





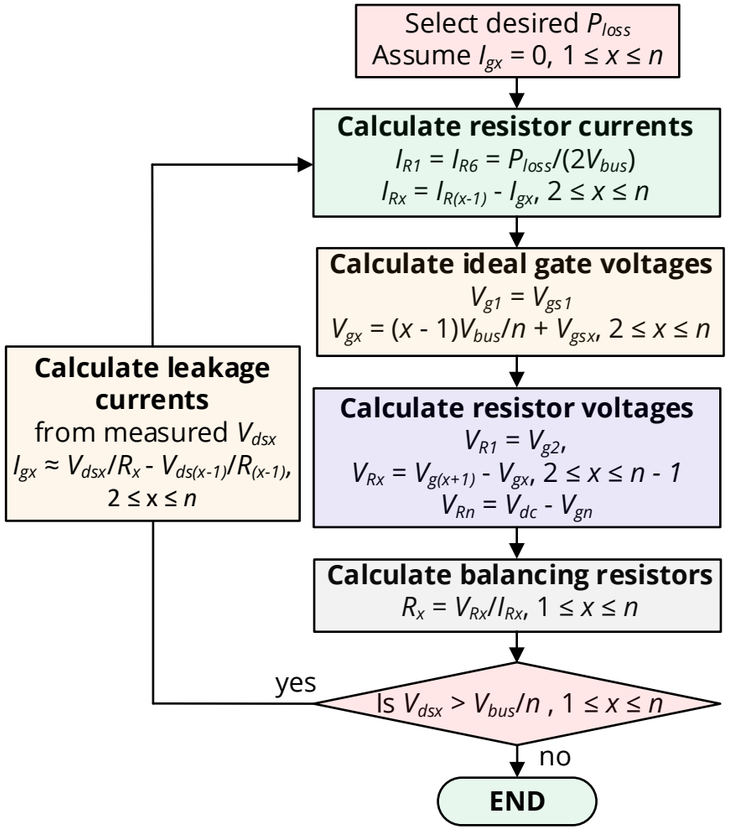
Normally-off cascaded switch prototype.



7.5kV/67μF capacitor bank.

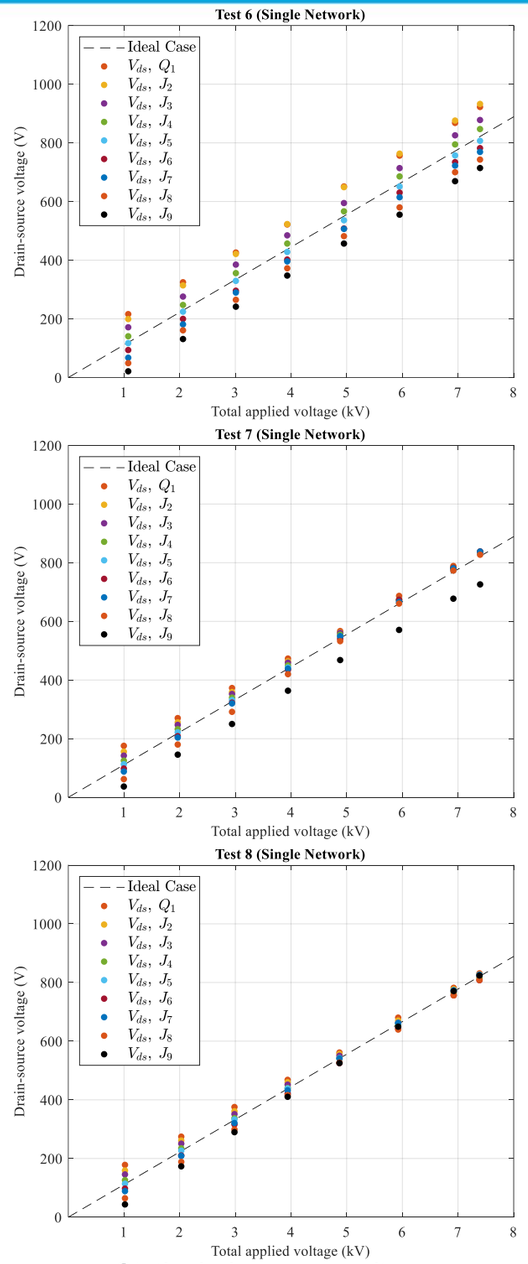
Static Voltage Balancing Procedure

- Hardware iterations estimate gate leakage current by measuring transistor drain voltages.
- Static balancing was optimized around 7.5kV.
- Total resistor balancing network power dissipation set to <3W.



Implemented Balancing Resistors			
	Test 6	Test 7	Test 8
R_1	2.199 MΩ	1.570 MΩ	1.562 MΩ
R_2	2.339 MΩ	1.639 MΩ	1.633 MΩ
R_3	2.317 MΩ	1.704 MΩ	1.698 MΩ
R_4	2.282 MΩ	1.734 MΩ	1.719 MΩ
R_5	2.313 MΩ	1.817 MΩ	1.817 MΩ
R_6	2.190 MΩ	1.785 MΩ	1.766 MΩ
R_7	2.395 MΩ	1.932 MΩ	1.912 MΩ
R_8	2.397 MΩ	1.987 MΩ	1.991 MΩ
R_9	2.491 MΩ	1.844 MΩ	2.103 MΩ

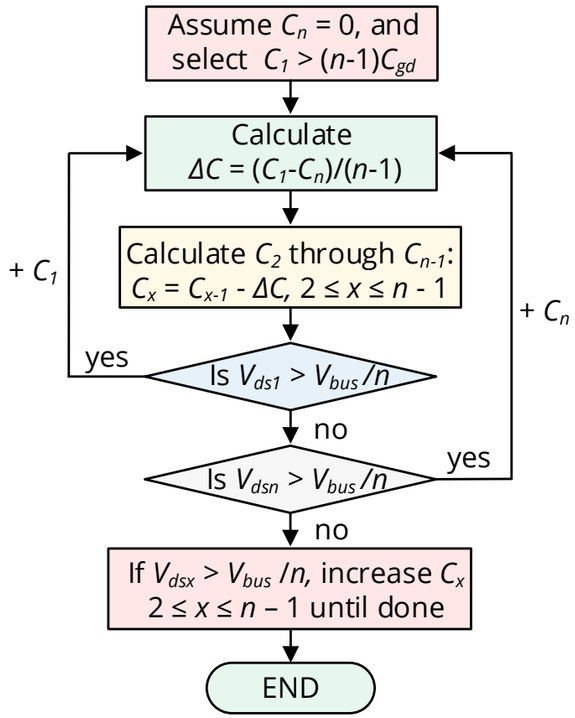
Voltage Error at 7.5kV			
	Test 6	Test 7	Test 8
V_{ds1}	12.2%	1.5%	1.3%
V_{ds2}	13.5%	1.3%	0.8%
V_{ds3}	6.8%	1.4%	-0.1%
V_{ds4}	3.1%	1.8%	-0.7%
V_{ds5}	-1.8%	0.9%	0.7%
V_{ds6}	-4.8%	2%	-1.6%
V_{ds7}	-6.4%	1.9%	0.6%
V_{ds8}	-9.6%	0.6%	-1.5%
V_{ds9}	-13%	-11%	0.4%



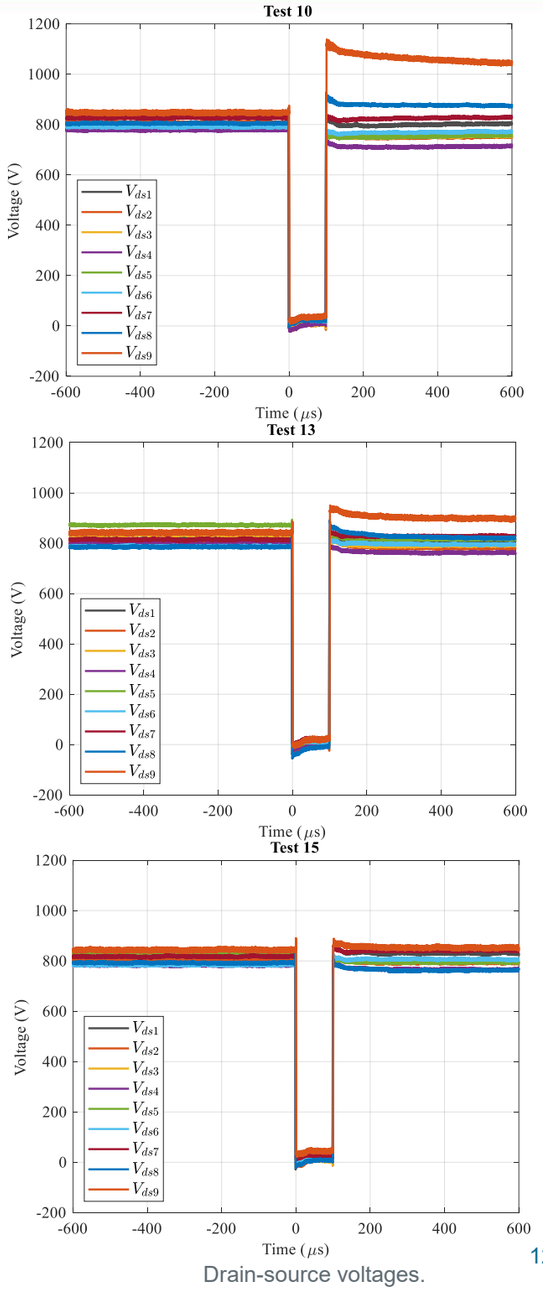
Static drain-source voltages.

Dynamic Voltage Balancing Procedure

- Dynamic balancing was achieved by tuning C_1 first, followed by C_9.
- The minimum C_1 value was selected based on C_{gd} and the number of series-connected devices.
- With $C_9 = 0$, C_1 was increased until V_{ds1} showed no overshoot.
- Intermediate capacitor values were evenly spaced by ΔC to support synchronized switching.
- C_1 was then held constant while C_9 was increased until no overvoltage appeared across V_{ds9}.



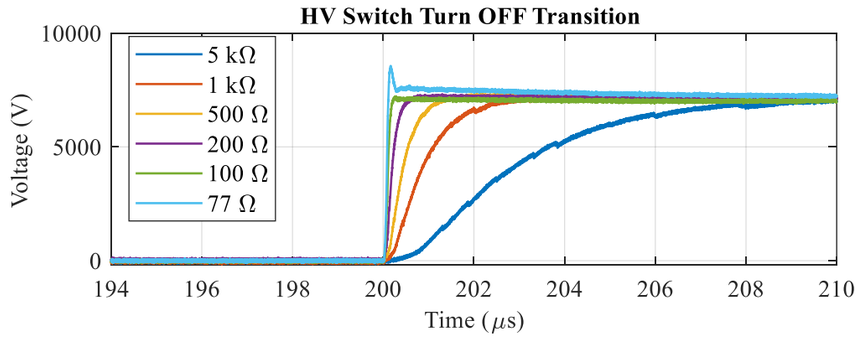
Implemented Balancing Capacitors						
	Test 10	Test 11	Test 12	Test 13	Test 14	Test 15
C_1	7n	7n	8n	9n	9n	9n
C_2	6.225n	6.25n	7.25n	8.25n	8.25n	8.25n
C_3	5.45n	5.5n	6.5n	7.5n	7.5n	7.5n
C_4	4.675n	4.75n	5.75n	6.75n	6.75n	6.75n
C_5	3.9n	4n	5n	6n	6n	6n
C_6	3.125n	3.25n	4.25n	5.25n	5.25n	5.25n
C_7	2.35n	2.5n	3.5n	4.5n	4.5n	4.5n
C_8	1.575n	1.75n	2.75n	3.75n	3.75n	4.23n
C_9	0.80n	1n	2n	3n	3.41n	3.41n

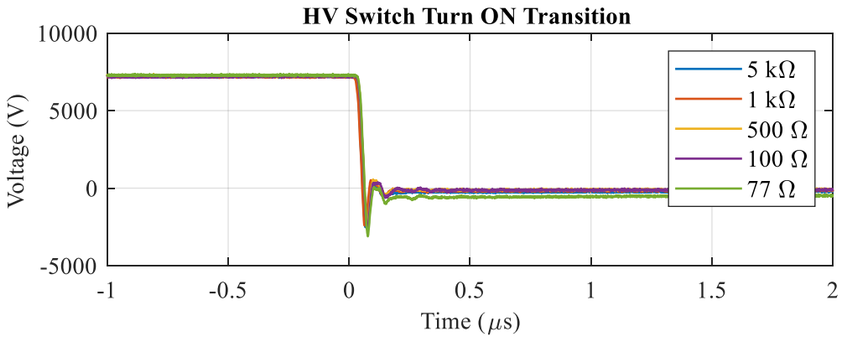


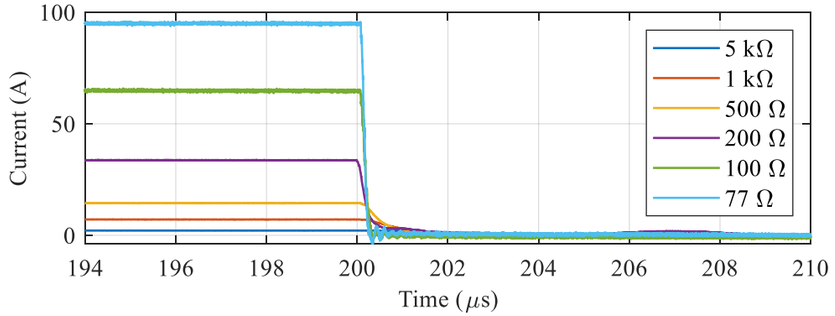
Drain-source voltages.

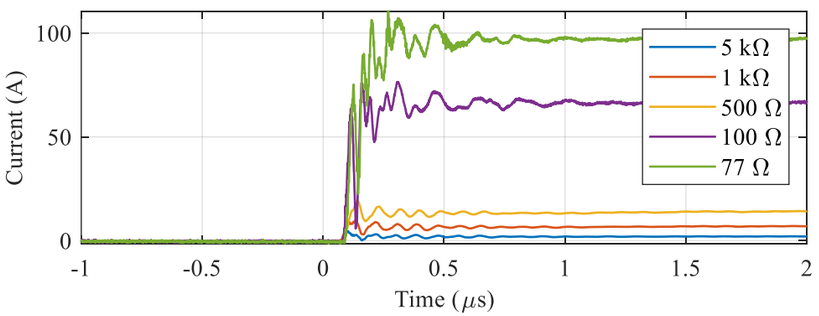
Turn ON and OFF Switching Performance

- High-voltage cascaded switch was tested at 7.5kV with resistive loads up to 100A.
- Turn-off transition time decreased as current increased, from approximately 5.5µs at 1.5A to 150ns at 100A.
- The turn-on speed is consistently fast across load conditions, with measured transition times of 50-100 ns for loads between 1.5A and 97A.
- Fast high-current turn-off supports SSCB operation by reducing fault-clearing time and limiting fault energy before device or system limits are exceeded.



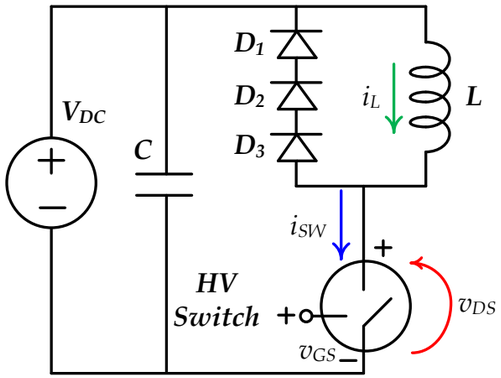




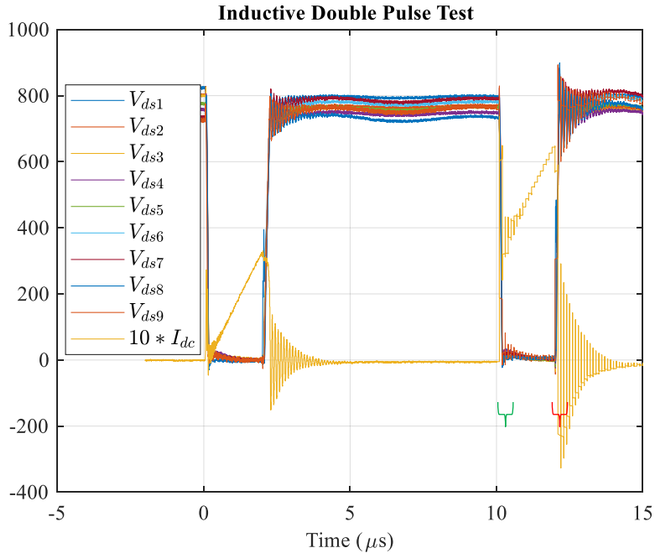


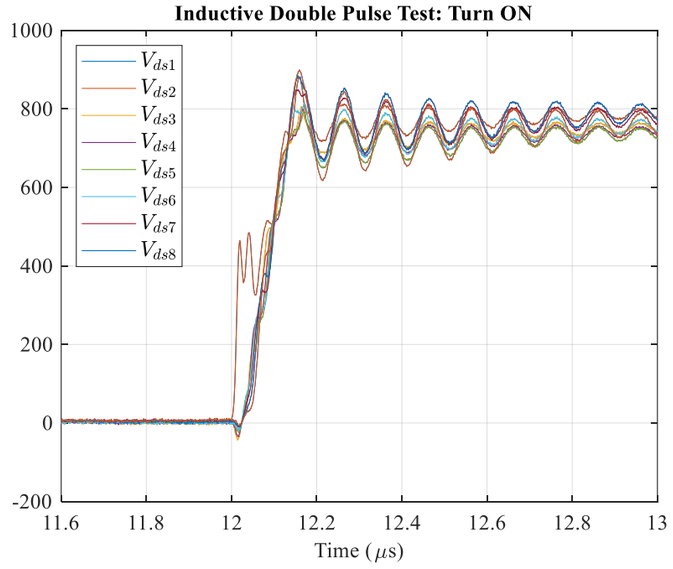
Inductive Double Pulse Test

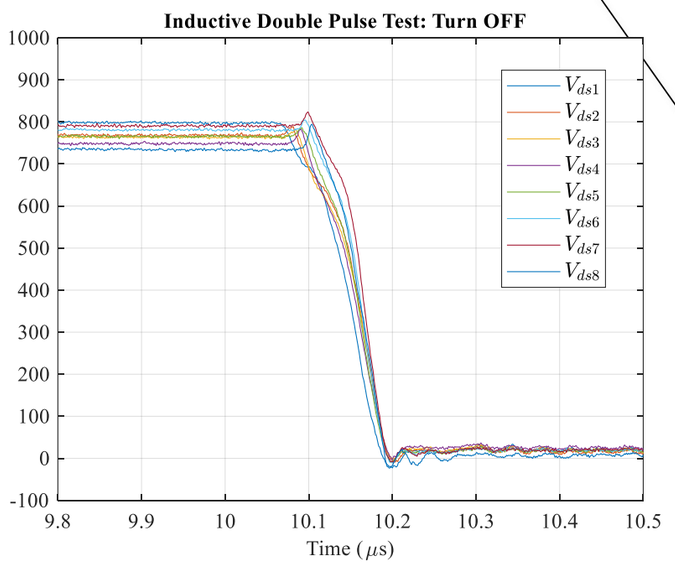
- A double-pulse test (DPT) circuit was used to characterize the switching performance of the cascaded high-voltage switch under inductive load conditions at 7kV.
- The high-voltage diode was realized using three series-connected 3.3 kV GC50MPS33H GeneSiC SiC Schottky diodes.
- Static and dynamic voltage sharing were maintained across the series-connected devices, ensuring operation within their respective safe operating areas.
- R_{gMOSon} = 20Ω, $R_{gMOSoff}$ = 2.35 Ω, R_{gJFET} = 20Ω.



Inductive DPT Circuit









Conclusions and Impact

- A high-voltage cascaded switch architecture was developed and experimentally evaluated for MVDC solid-state circuit breaker applications.
- Static voltage balancing was successfully achieved near 7.5 kV, with the resistor balancing network constrained to less than 3 W total power dissipation.
- Double-pulse testing demonstrated reliable switching performance under inductive load conditions, with static and dynamic voltage sharing maintained across the series-connected devices.
- Resistive-load testing at 7.5 kV and up to 100 A showed fast switching behavior, including turn-off transition times as low as approximately 150 ns at high current.
- The demonstrated fast turn-off capability can directly benefit SSCB operation by reducing fault-clearing time, limiting fault energy, and lowering electrical and thermal stress on system components.

Future Directions/ Next Steps

- ❑ Experimentally evaluate the complete SSCB protection architecture, including the normally-on path, normally-off capacitor-assisted branch, and MOV clamping branch.
- ❑ Optimize the capacitor and MOV sizing to limit voltage overshoot, control dv/dt, and ensure safe energy absorption during interruption events.
- ❑ Design and integrate a complete SSCB module that combines the normally-on, normally-off, and MOV branches into a single hardware platform.
- ❑ Improve integration and packaging to minimize parasitic inductance, reduce voltage overshoot, and enhance dynamic voltage sharing across the cascaded switch.
- ❑ Develop system-level MVDC protection coordination strategies, including fault detection, gate-drive timing, commutation control, and breaker recovery after interruption.
- ❑ Extend testing to higher fault currents and higher stored-energy conditions to verify device safe operating area margins and validate scalability.

Questions?

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