Presentation Submission Information

- Presentation ID: 4.3
- Presentation Title: Medium-voltage Alternating Current-to-Direct Current (AC-to-DC) Versatile Energy Router with Integrated Conversion (MAVERIC)
- Authors: Ian Webb, Adel Nasiri
- Organizations: Savannah River National Laboratory, University of South Carolina

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Medium-voltage AC-to-DC Versatile Energy Router with Integrated Conversion (MAVERIC)

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DOE OE TRAC Peer Review 2026

U.S. DEPARTMENT of ENERGY

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BSRA Battelle Savannah River Alliance, LLC

Project Overview

Medium-Voltage **A**C-to-DC **V**ersatile **E**nergy **R**outer with **I**ntegrated **C**onversion (MAVERIC)

- **Technology Area:**
  Advanced Transformers, Advanced Power Electronics
- **Strategic Pathway Alignment:**
  - **Optimize:** Utilizing 3.3 kV (kilovolt) devices and advanced topologies, MAVERIC offers a power density of 0.8 kW/L (kilowatt/liter) end-to-end and dramatically reduces conversion loses for large DC loads.
  - **Grow:** MAVERIC is a modular and scalable solution to a modern grid problem, creating a bridge between existing medium voltage AC grids and emerging 800VDC systems.

Project Description:
Development, validation, and commercialization of a modular 420kVA (kilovolt-amperes) AC/DC converter for MV (medium voltage) DC distribution

Period of Performance:
1 OCT 2025 – 30 SEP 2027

Award Amount:
$1,200,000

Prime Awardee:
Savannah River National Laboratory (SRNL)

Partners:
University of South Carolina (UofSC)
Santee Cooper

Why is the Medium Voltage Solid-State Transformer (MV SST) Needed?

- MV and HV (high voltage) DC converter stations are costly, inflexible, overly proprietary, and lack modularity, driving poor interoperability between vendors and scale.
- DC converter substation cost is driven largely by:
  - Cost of Balance of System (BOS) (cables, conduits, switchgear, installation/commissioning time)
  - Low power density
  - Project-specific design tailoring (non-standardized hardware performance requirements)
  - Poor interoperability between converter substation assets
  - Short lifespan
- Data centers
- Grid level energy storage
- Power level at 480VAC is not sufficient for modern sources, loads, and storage.

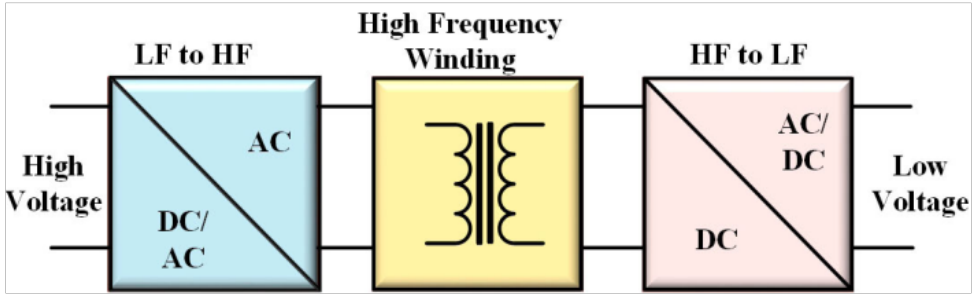


Figure 1: SST Functional Block Diagram

Technical Innovation

- MAVERIC: 15kVAC class bidirectional DC converter capable of 3.8MVA @ 800VDC output
- Modular design- constructed with several 210kW modules
- Power density: 0.8kW/L (end-to-end)
- System efficiencies as high as 98.5%
- Based on new-generation 3.3kV high-speed devices- huge upgrade from standard 1.2 - 1.7kV technologies.

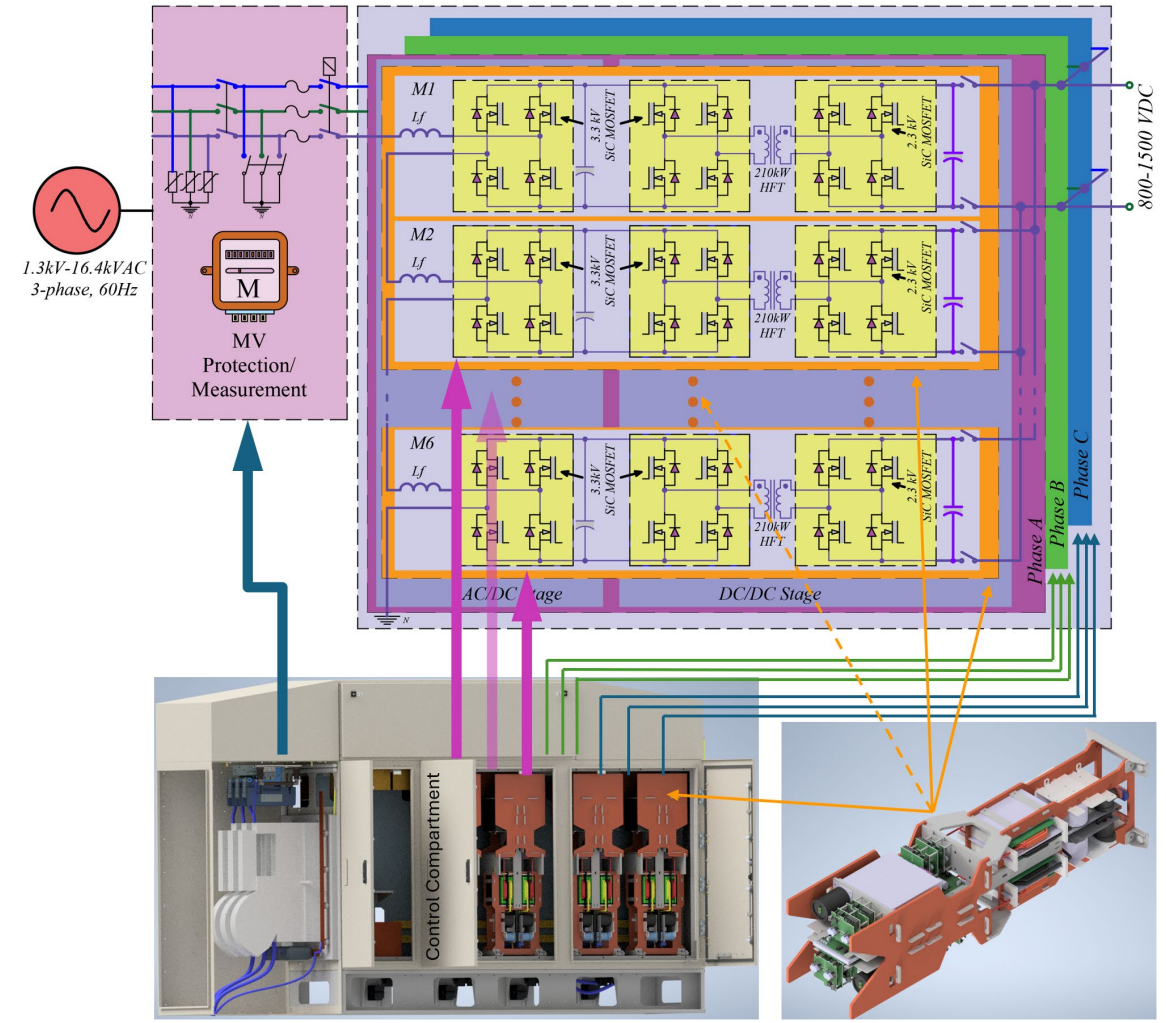


Figure 2: Topology of MAVERIC system

Technical Innovation (Cont.)

- DC voltage adjusts at very high bandwidth (10kHz (kilohertz)) to meet DC distribution dynamics.
- Each H-bridge employs a high frequency transformer (20-30kHz) that utilizes advanced magnetic materials (ferrite cores, Litz wires).
- Resonant operation reduces electrical stresses on components, losses, and minimizes electromagnetic interference.
- Relies on quadruple control: primary and secondary duty cycles, frequency modulation, and phase-shift control
- Testing will occur at the SRNL Medium Voltage Test Bed: a solid-state transformer-based medium voltage (0-13.8kV) testing capability
- Grid Compliance- comprehensive review of relevant grid codes (IEEE 1547, UL 347A, IEEE 519), interconnection standards, and utility policies, summarized in a Control Requirements Document

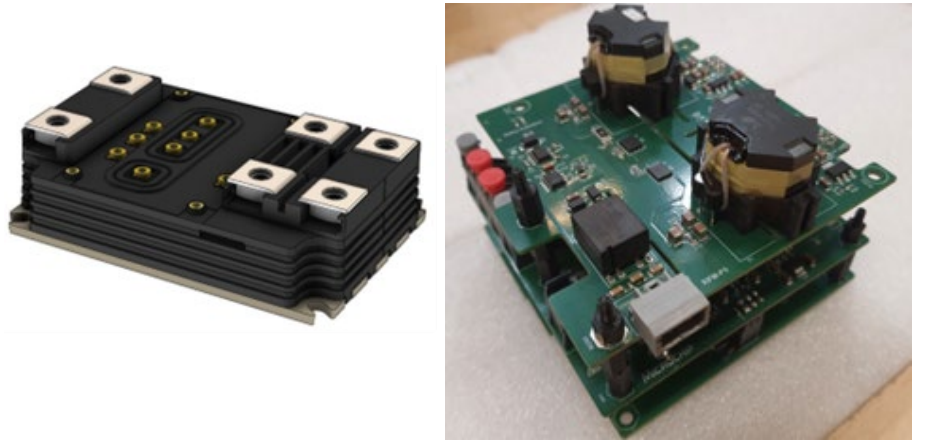


Figure 3: 374A, 3.3kV MOSFET switch with the associated gate driver.

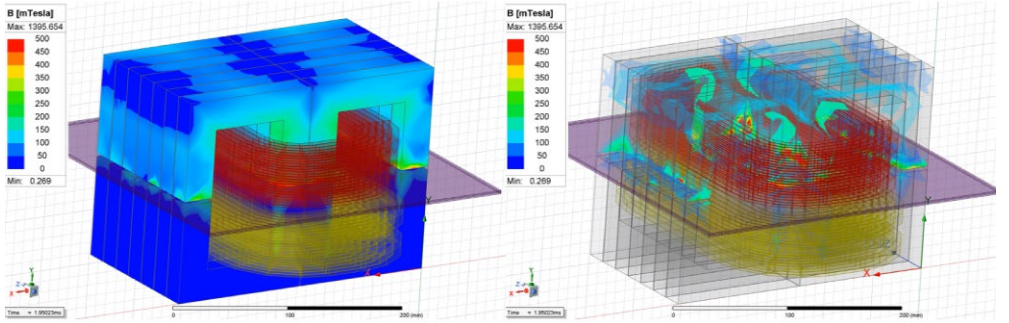


Figure 4: High frequency transformer flux modeling

Converter Module Development

Converter Module Development

CAD (computer-aided design) model detailing the physical layout of converter switches, gate drivers, transformer placement, cold plates, and all other relevant components completed

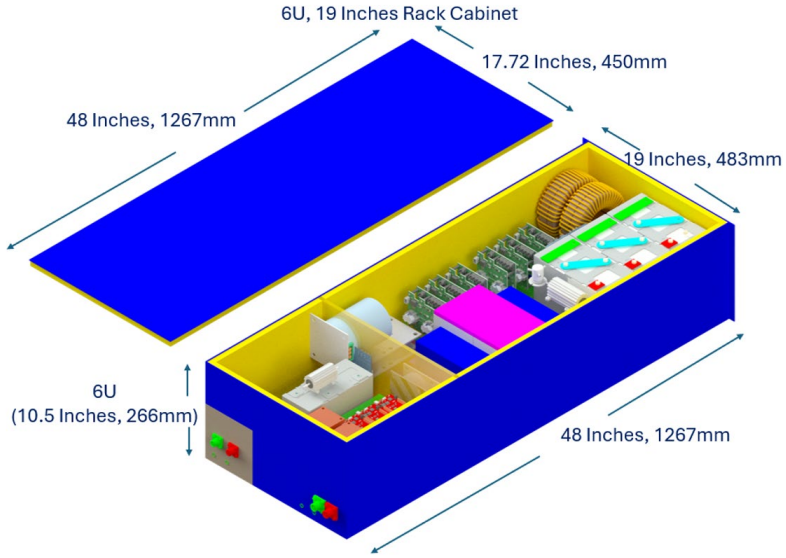
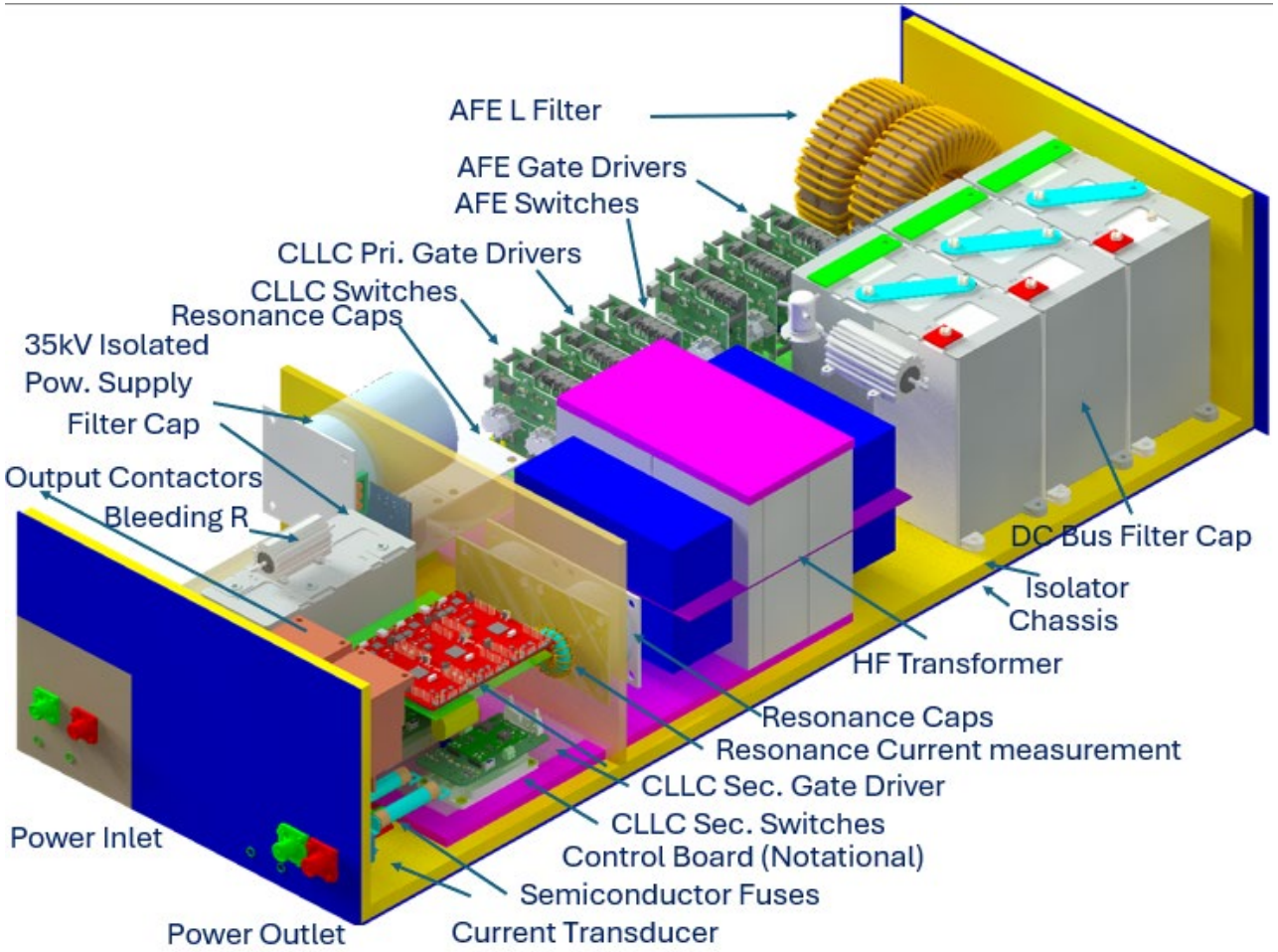


Figure 9: MAVERIC module in enclosure



*AFE – Active front end

Figure 10: MAVERIC module with item callouts

Converter Module Development (Cont.)

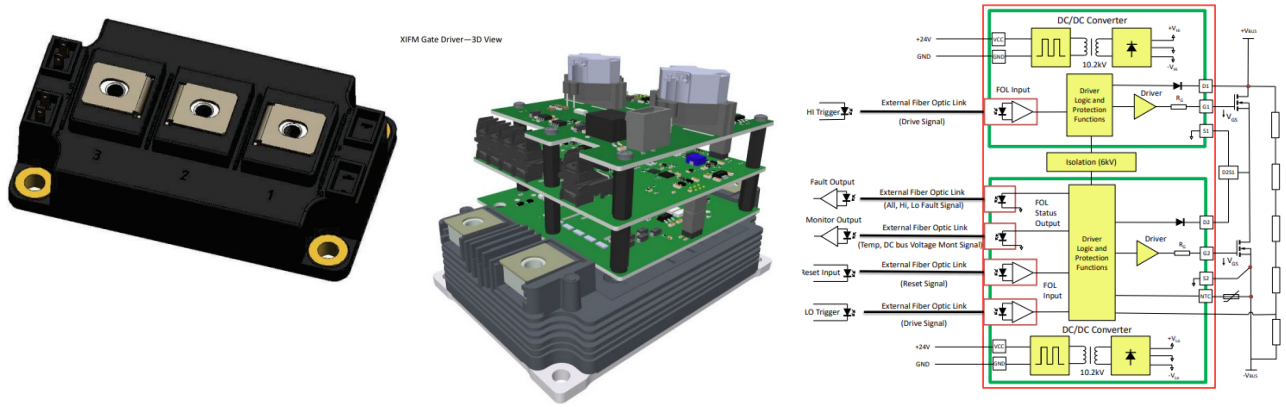


Figure 11: Switch and gate driver renderings

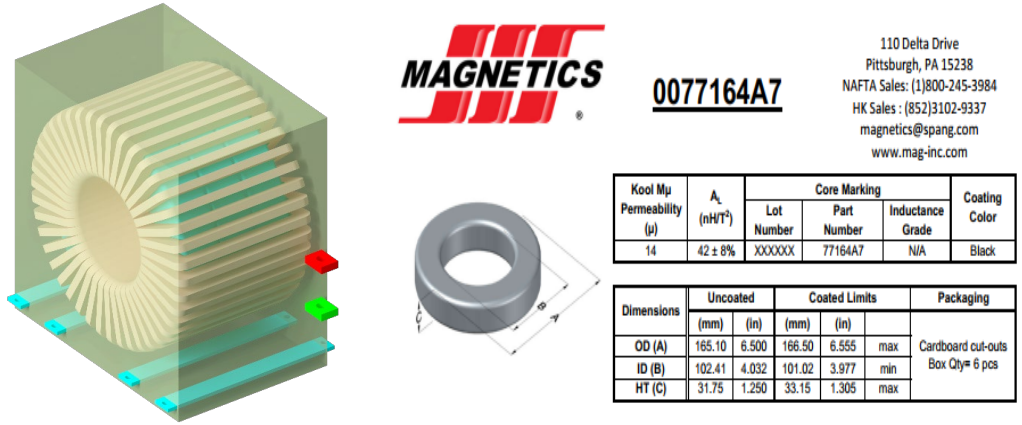


Figure 12: Inductor material renderings

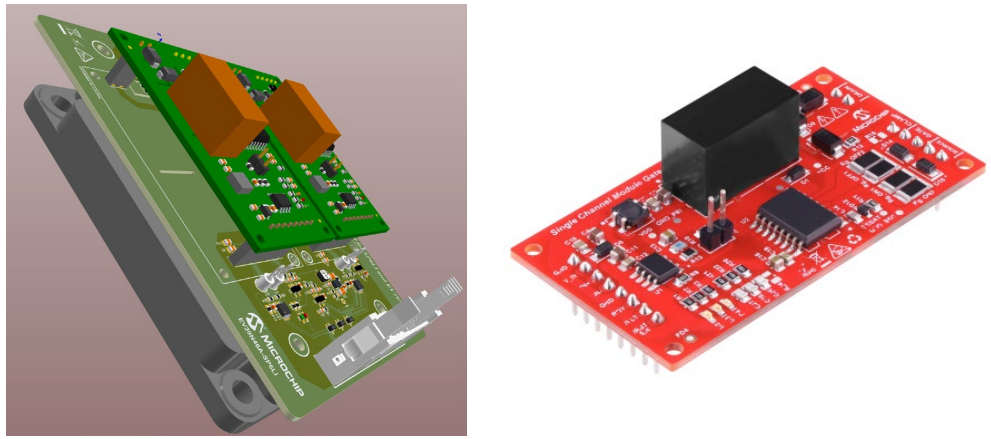


Figure 13: Gate Drive Board and Adapter Board

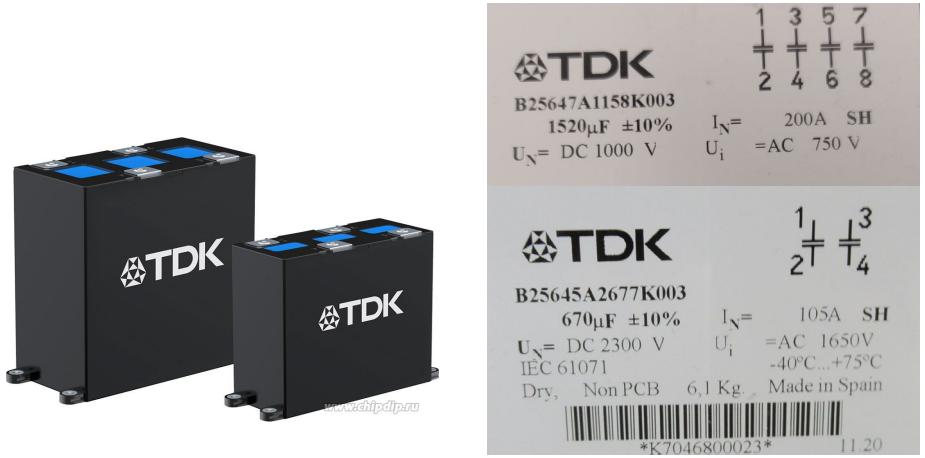


Figure 14: DC bus capacitors (AFE-bottom, CLLC-top)

Converter Module Development (Cont.)

Double Pulse Testing of 3.3kV switches (2000V, 28A)

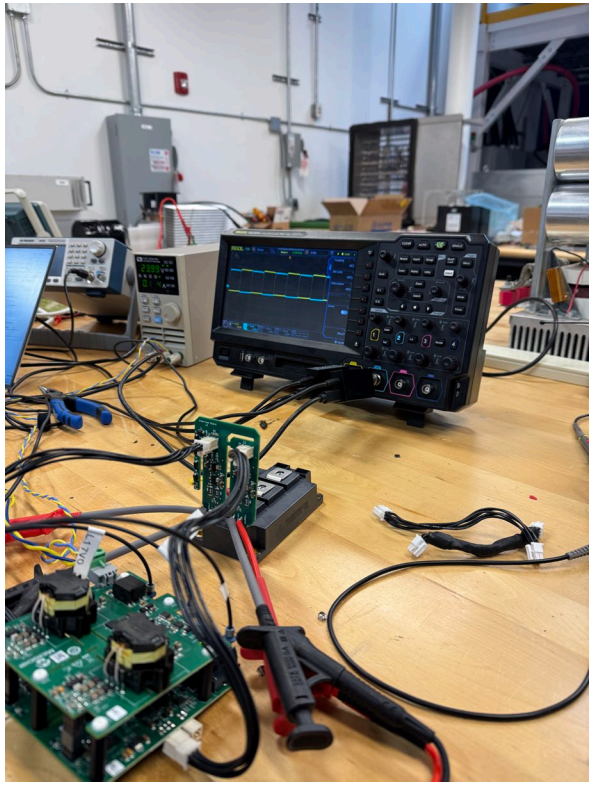
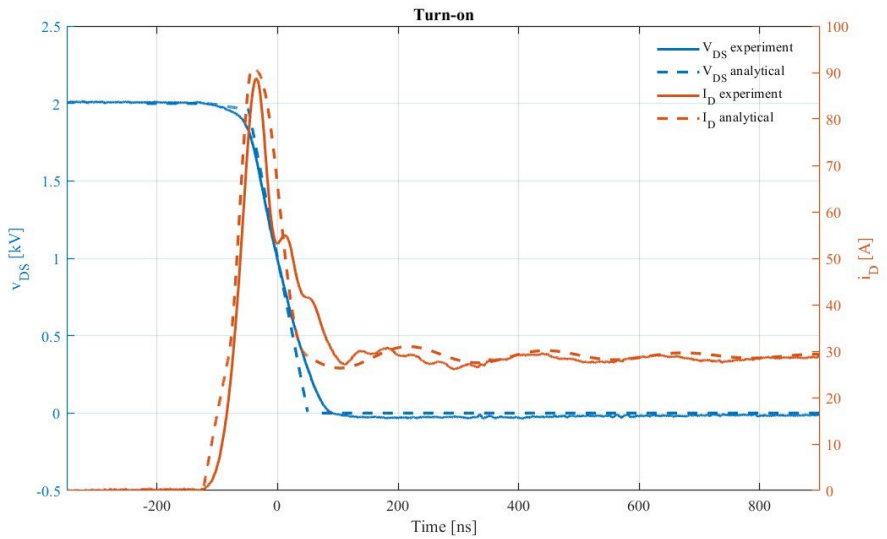
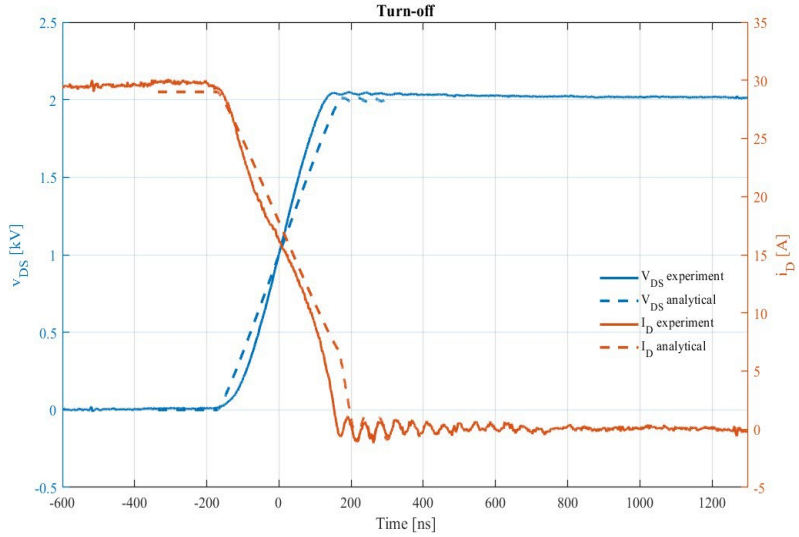


Figure 15: Gate driver test setup





	Experiment	Analytical
E_{on_mJ}	10.179	12.302
E_{off_mJ}	3.4461	4.8055
$Ipeak_{on}$	88.737	92.004
$Vpeak_{off}$	2050.9	2011.6

Figure 16: Turn-on characteristic (top left), turn-off characteristic (top right), experimental vs analytical characteristics (bottom)

Bus Bars and Cold Plates

Bus Bar and Cold Plate Development

Primary side, secondary side, and capacitor bus bar/cold plate design has been completed, being manufactured now

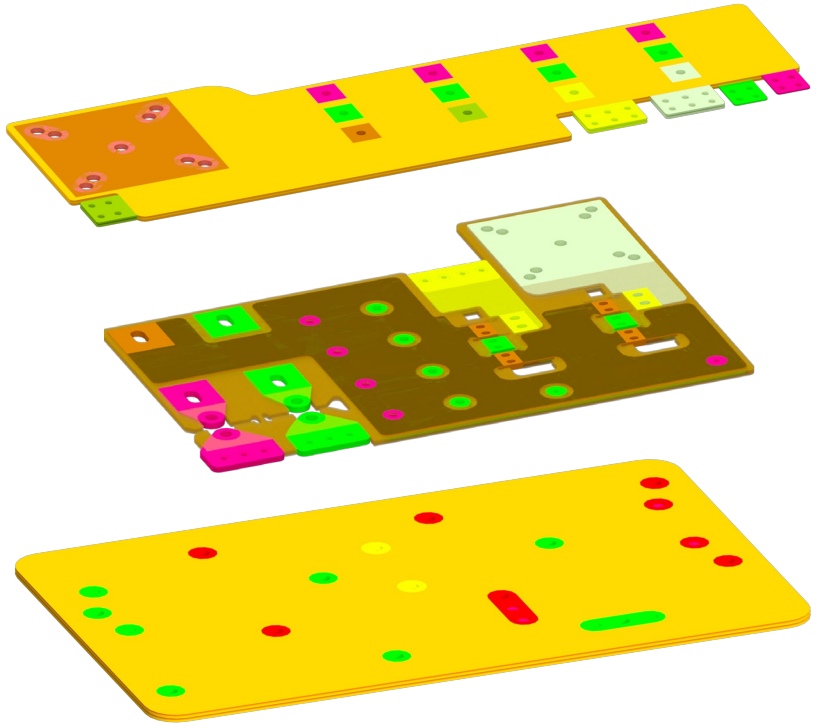


Figure 17: Primary side busbar (top), secondary side busbar (middle), capacitor busbar (bottom)

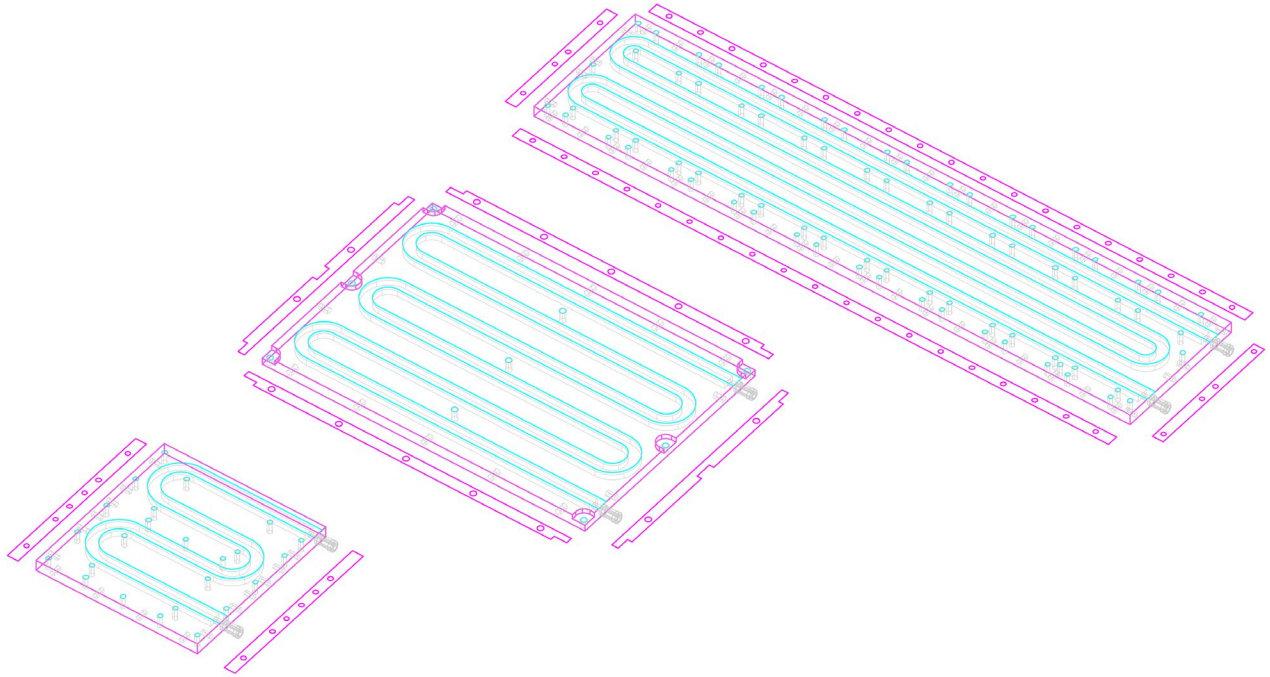


Figure 18: Secondary side cold plate (left), transformer cold plate (middle), primary side cold plate (right)

Converter Controller Development

Converter Controller Development

- Responsible for coordinating control for one single-phase AFE (active front end) stage and two bi-directional CLLC DC-DC converter
- Receives feedback in the form of input/output voltages and currents, DC-link quantities, and cold-plate temperature from primary and secondary sides
- Sends digital input/output commands, PWM-related (pulse-width modulation) signals, and gate commands via fiber optic signaling

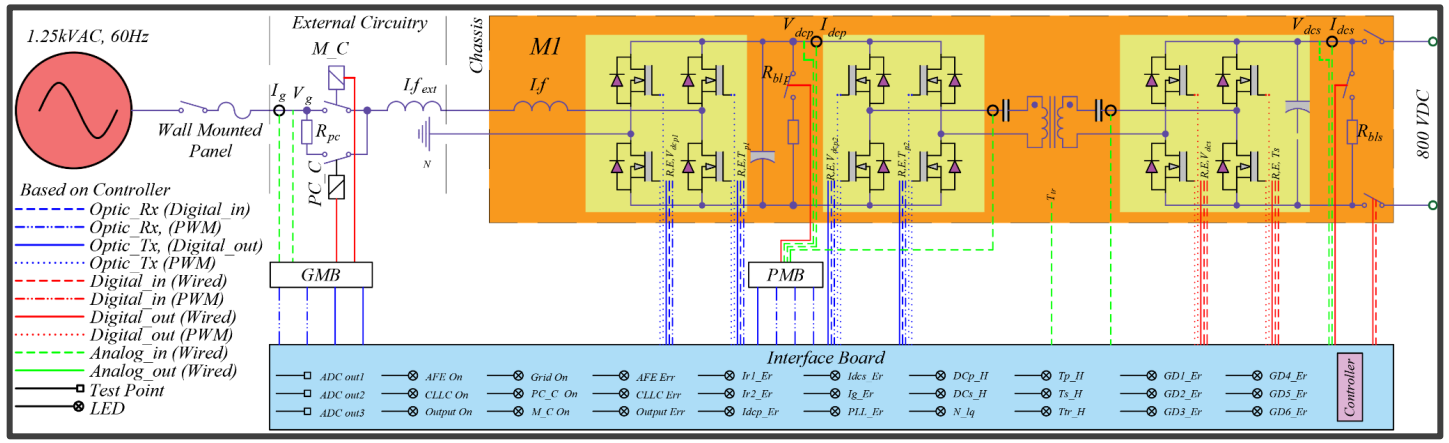


Figure 19: Controller interface with converter hardware

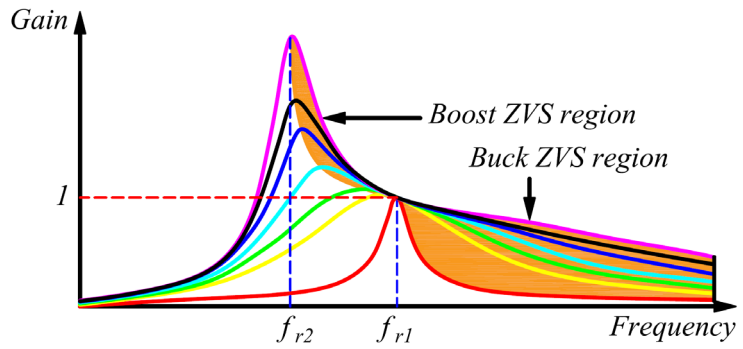
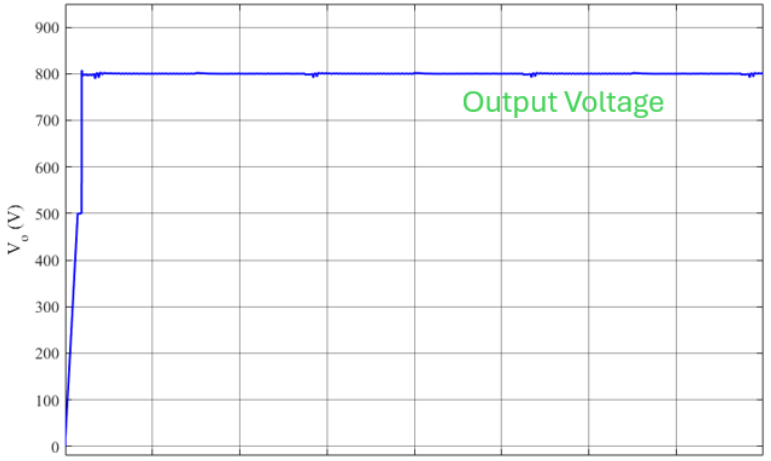


Figure 20: CLLC operating regions

Converter Controller Development (Cont.)

- Simulation of both AFE and CLLC resonant converter architecture successfully simulated
- Load profile closely mimics data center draw during model training



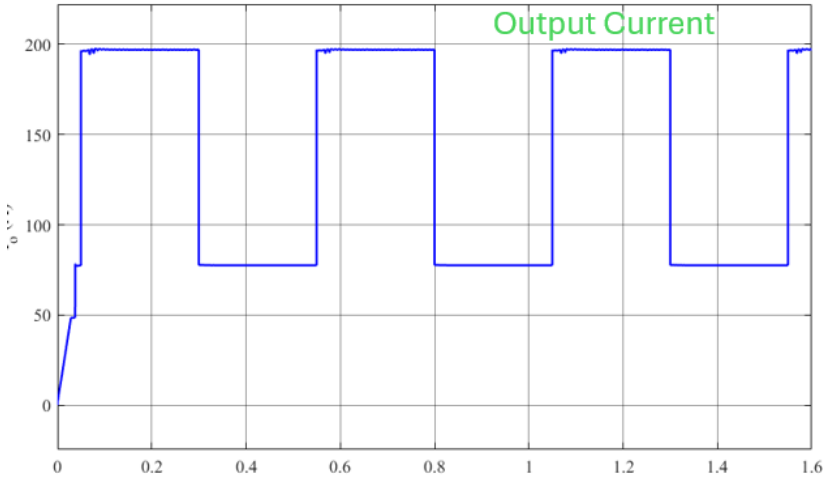


Figure 21: AFE + CLLC simulation output voltage (left) and output current (right)

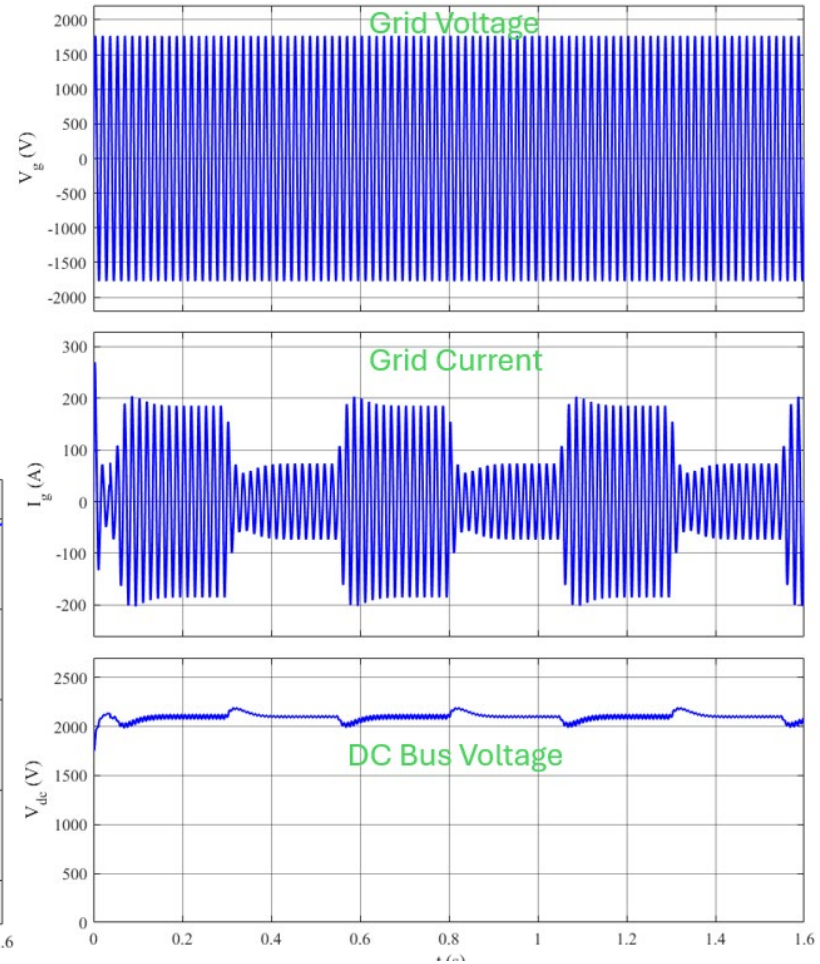


Figure 22: AFE + CLLC simulation grid voltage (top), grid current (middle), and DC bus voltage (bottom)

Converter Controller Development (Cont.)

- FPGA (Field-programmable gate array) controller section for control logic, PWM generation, monitoring, sequencing, and communication
- Fiber-optic receiver channels for digital feedback and status signals from the converter
- Fiber-optic transmitter channels for digital output and PWM/gate-command signals to the converter
- Contactor/relay status feedback inputs
- Ethernet and serial communication/service interfaces
- Board-level power input, protection, and DC/DC regulation

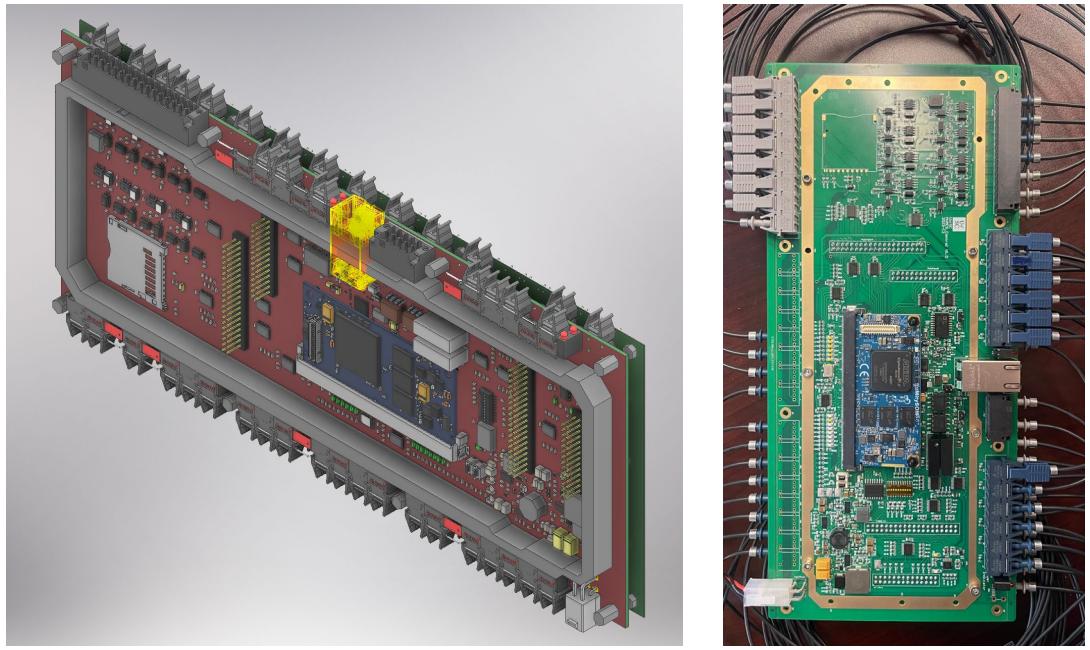


Figure 23: Converter controller rendering (left) and actual board (right)

Converter Controller Development (Cont.)

Controller Human-Machine Interface (HMI) allows users to adjust controller parameters, observe important SST variables, and monitor system status during converter operation

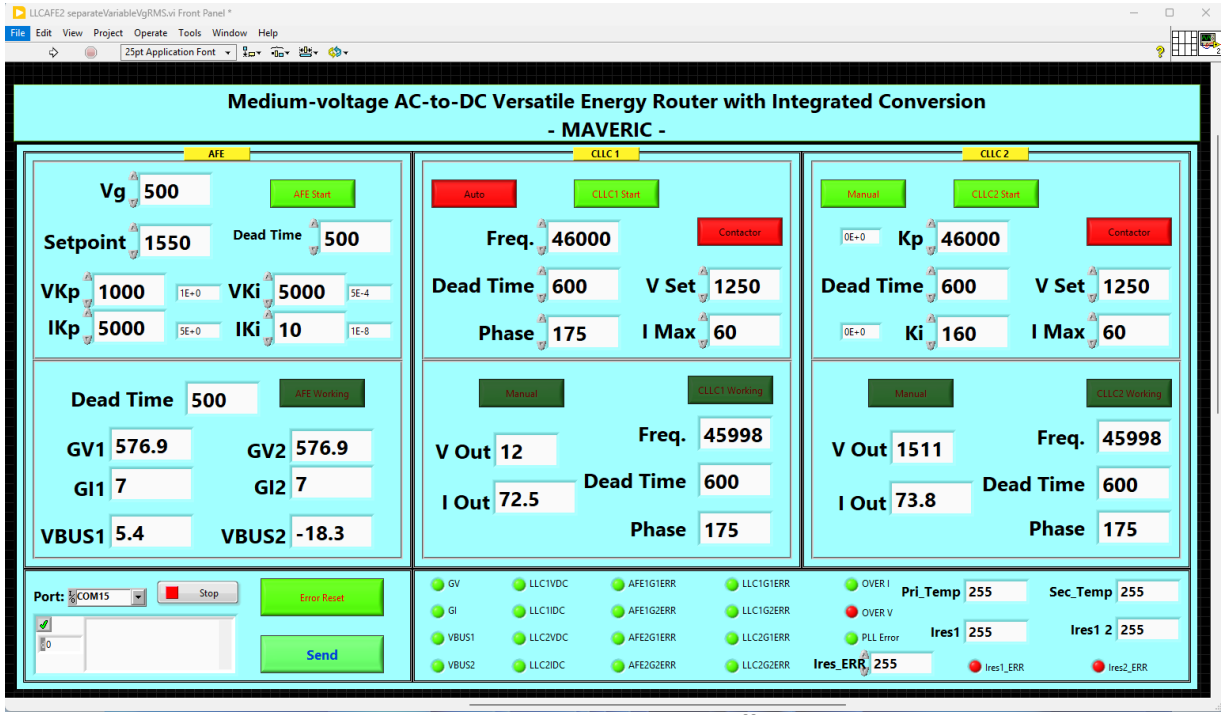


Figure 24: Converter controller HMI

Medium Frequency Transformer Development

Medium Frequency Transformer Development (Cont.)

MF (medium frequency) transformer design is complete, and manufacturing has started.

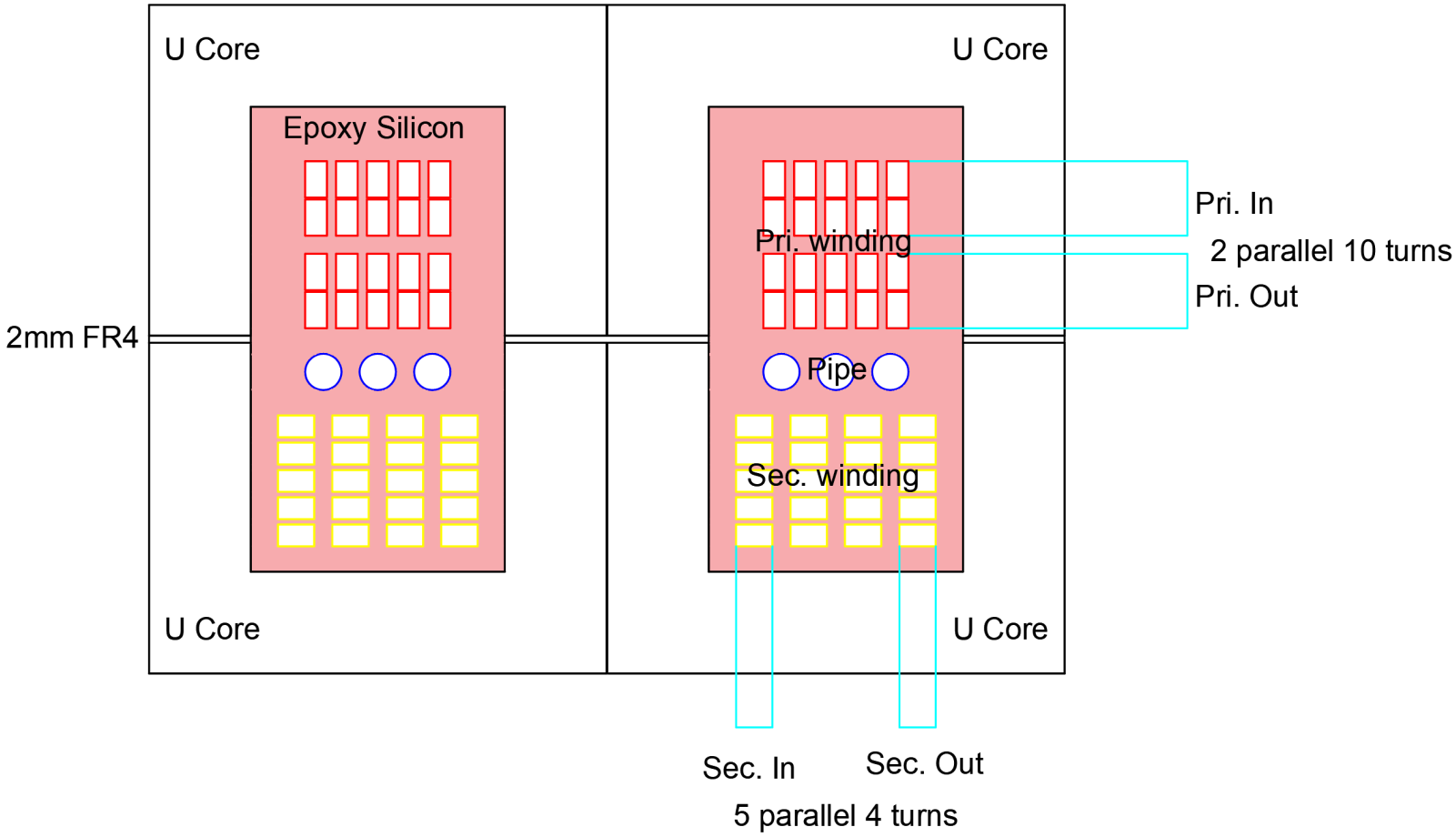


Figure 25: Cross section of medium frequency transformer

Medium Frequency Transformer Development

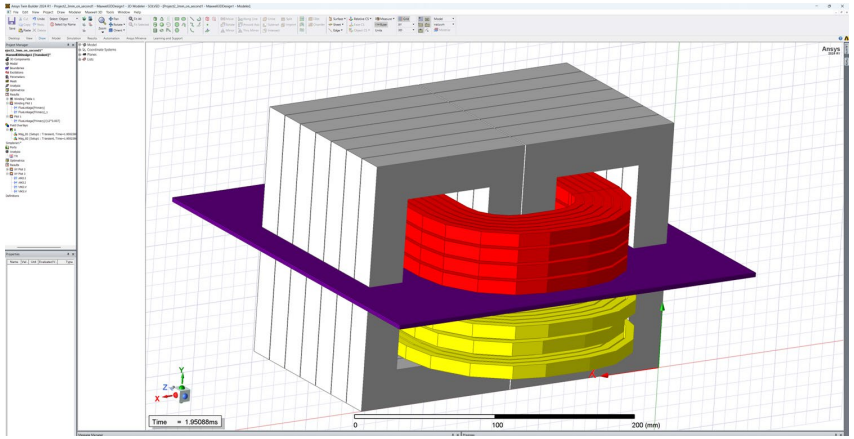


Figure 26: CAD rendering of medium frequency transformer

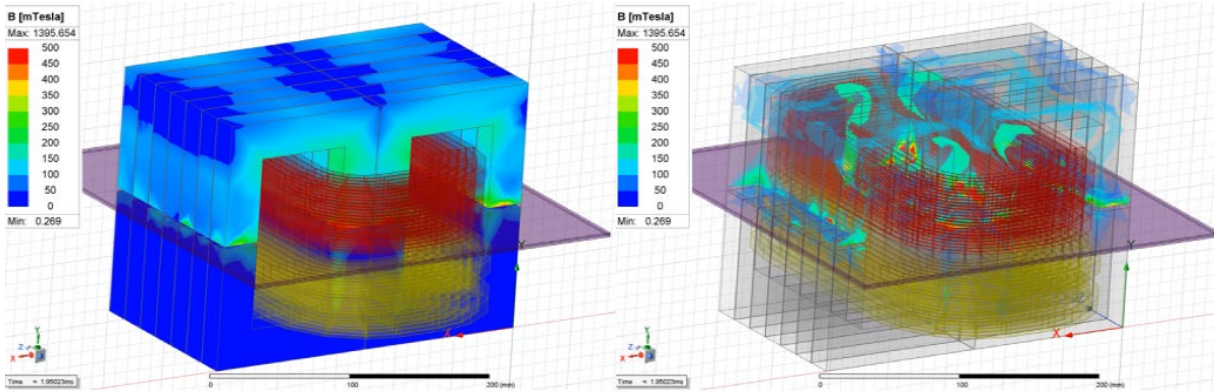


Figure 27: Magnetic field intensity distribution simulation of medium frequency transformer

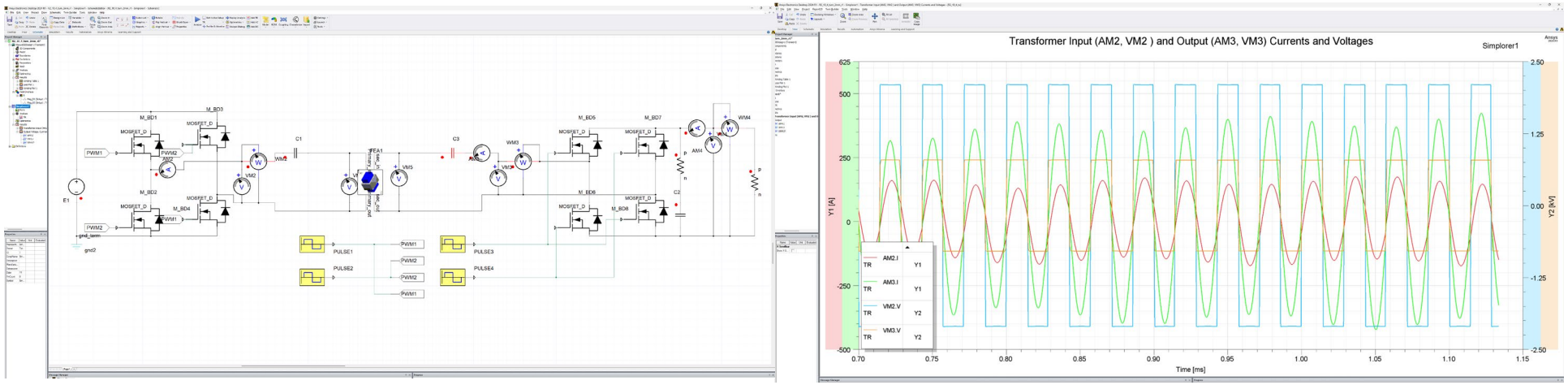


Figure 28: Ansys multi-physics circuit simulator (left) and operating waveforms (right)

Medium Frequency Transformer Development (Cont.)

MF transformer design is complete, and manufacturing has started.

Spec	Value	Unit	
L-L Grid Voltage	34.5	kVAC	
Phase Voltage	20	kVAC	
Required Isolation Voltage (min)	42	kVAC (60 Sec)	60kV peak
Required Continuous Isolation Voltage	22	kVAC	31kV peak
Switching Frequency Min	35	kHz	
Switching frequency Max	50	kHz	
DC link Voltage	2100	VDC	
Cell output Voltage	800	VDC	
Turns Ratio	0.4		
Number of turn	10/4	turns	
Rated Power	210	KW	
Duration	100%	Continuous	
Termination	Flying Leads or Multilayer Busbar		Please see the drawing for termination
Partial Discharge Max	50pC at 1.8xVnom for 30 seconds stress test then 1.3xVnom for 180 seconds	Pico Columbs	Vnom refers to exposed grid voltage
Efficiency	>99.4	%	

Figure 29: Targeted operating specifications of medium frequency transformer

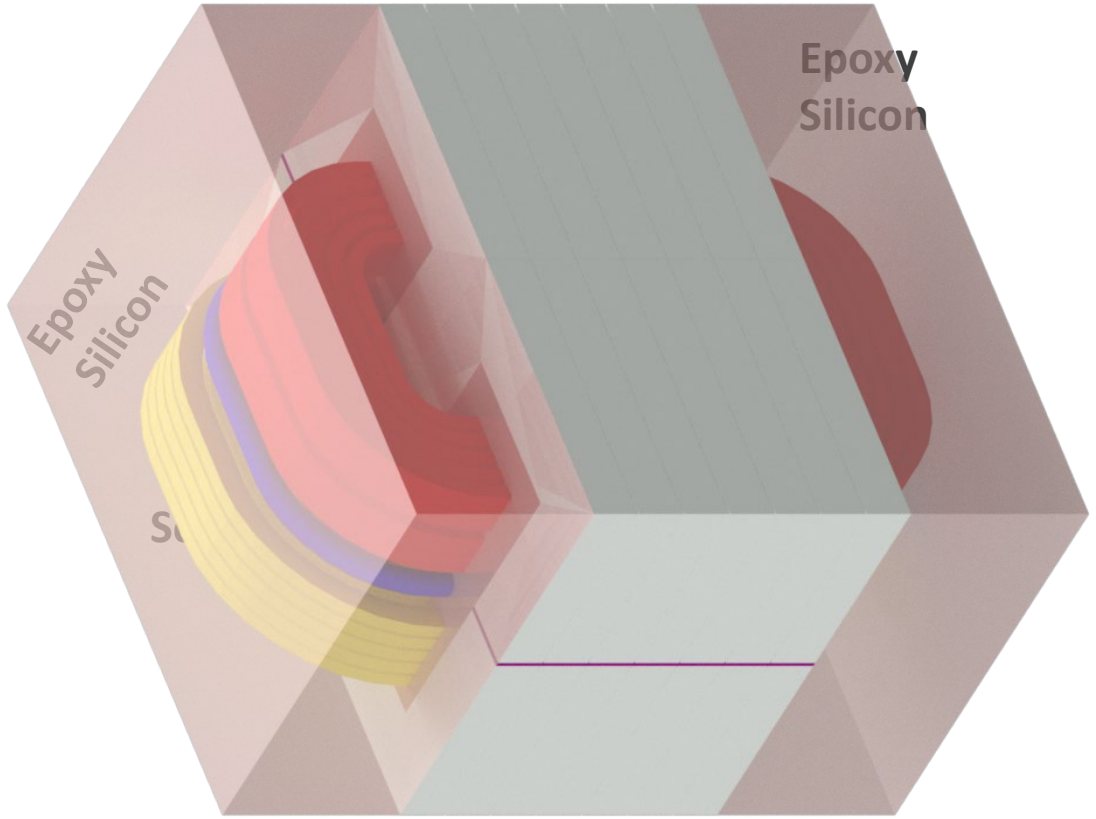


Figure 30: 3D rendering of medium frequency transformer

Controller Hardware-in-the-Loop Integration

Controller Hardware-in-the-loop Integration

Model confirmed to work in Simulink, work ongoing to port it to RT-LAB (OPAL-RT)

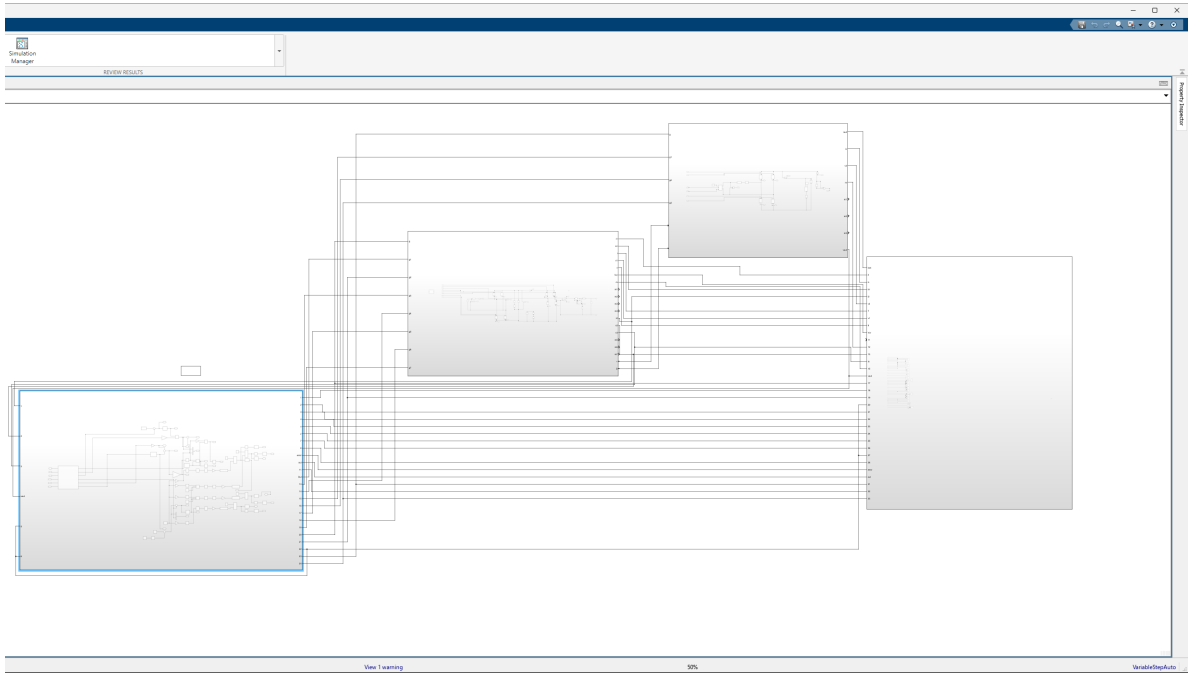


Figure 31: Simulink model of MAVERIC

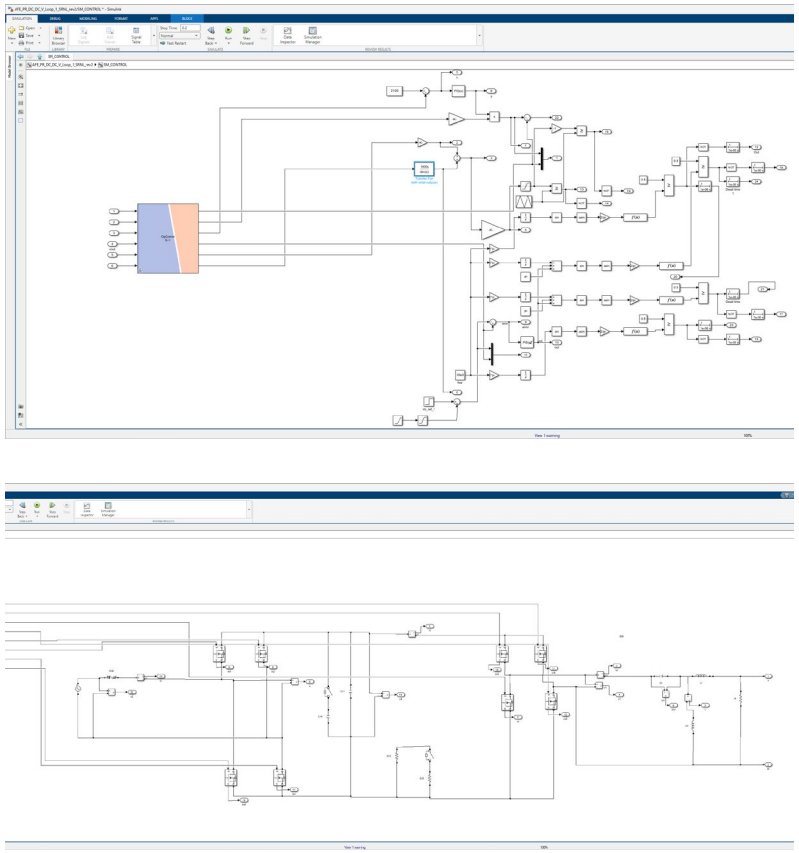


Figure 32: Select Simulink subblocks expanded

Future Direction and Next Steps

Next Steps

- Converter Module Development
  - Integrate both AFE and CLLC converters and perform energized tests
  - Integrate high frequency transformer
- Module Controller
  - Integrate controller with converter module
  - Continue to develop HMI
- Hardware-in-the-Loop Integration of MAVERIC controller
  - OPAL-RT/RT-LAB integration of converter controller
  - Analyze impact of grid disturbances on MAVERIC controller and grid support functions
- Test and Evaluation
  - Will perform testing at SRNL Medium Voltage Test Bed
- Preparation for full MAVERIC development and deployment

Acknowledgements

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