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- **Organization(s):**
  - Sandia National Laboratories,
  - North Carolina State University,
  - Hepburn and Sons

Sandia National Laboratories

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U.S. DEPARTMENT of ENERGY

DEMONSTRATION OF MODULAR 5-KV CLASS SOLID STATE POWER SUBSTATION

Jack Flicker[1], Jacob Mueller[1], Subhashish Battacharya[2], Vasishta Burugula[2], Richard Byron Beddingfield[2], Patrick Lewis[3], Hunter Gray[3], Anthony Popovski[3]

1. Sandia National Laboratories,
2. North Carolina State University,
3. Hepburn and Sons

DOE OE TRAC Peer Review 2026

Washington, DC September 21 – 22, 2026

U.S. DEPARTMENT of ENERGY NNSA

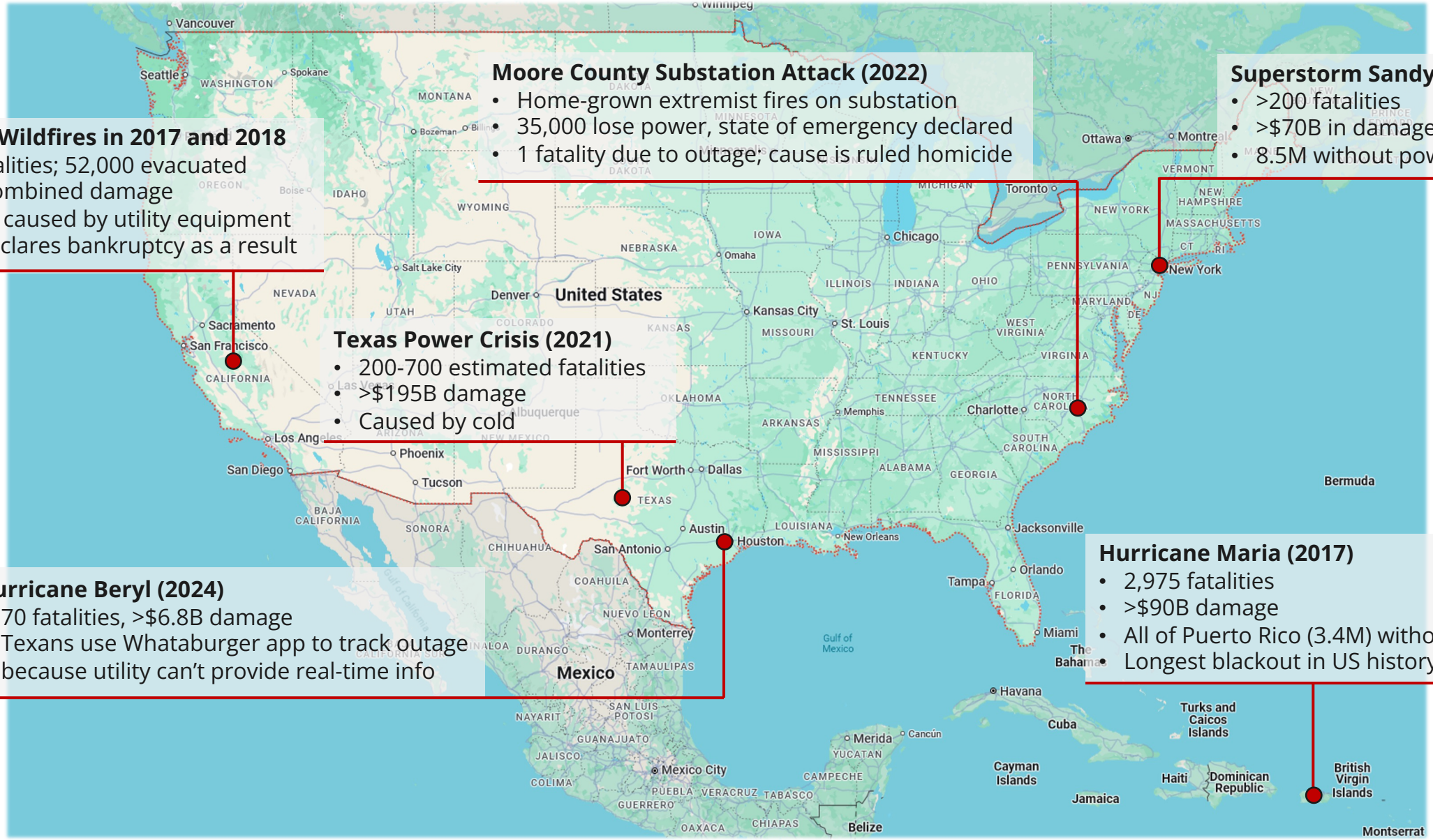
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PROJECT OVERVIEW

- **Project Description:** Modular, fault tolerant building blocks are required for Solid State Power Substation (SSPS) concepts to be reliable, manufacturable, and cost-effective and enable a paradigm shift in deployment. Lightweight and highly portable modules, assembled on site, provide significant value to rural and remote locations, compact urban environments, and disaster relief. This project is fabricating and demonstrating an operational SSPS interfacing a local area DC distribution system with a medium voltage AC utility grid. The system is composed of building block modules with 15kV-class isolation, optimized for weight/volume and production for rapid deployment in response to disasters and resource failures, and fault tolerant with redundant and self-recoverable control. The SSPS will be demonstrated experimentally in both normal and contingency operation in a laboratory single-phase, 4160V system.
- **Period of Performance:** 10/01/2025 to 09/30/2027
- **Award Amount:** $1,200,000 Federal Share
- **Prime Awardee:** Sandia National Laboratories
- **Partners:** Sandia National Laboratories, North Carolina State University (NCSU), Hepburn & Sons
- **Technology Area:** Advanced Power Electronics
- **Alignment/Supports strategic pathway:** This project **Optimizes** the grid by developing a Solid State Power Substation that can improve power quality, control power flow, and increase line capacity. This allows for a higher performing, more stable grid, especially for the integration of large electric loads. A modular, fault tolerant hardware scheme allows for lower cost, more robust operation when faced with contingencies

PROJECT DETAILS

PROBLEM STATEMENT



California Wildfires in 2017 and 2018
- >100 fatalities; 52,000 evacuated
- >$25B combined damage
- Fires are caused by utility equipment
- Utility declares bankruptcy as a result

Moore County Substation Attack (2022)
- Home-grown extremist fires on substation
- 35,000 lose power, state of emergency declared
- 1 fatality due to outage; cause is ruled homicide

Superstorm Sandy (2012)
- >200 fatalities
- >$70B in damage
- 8.5M without power

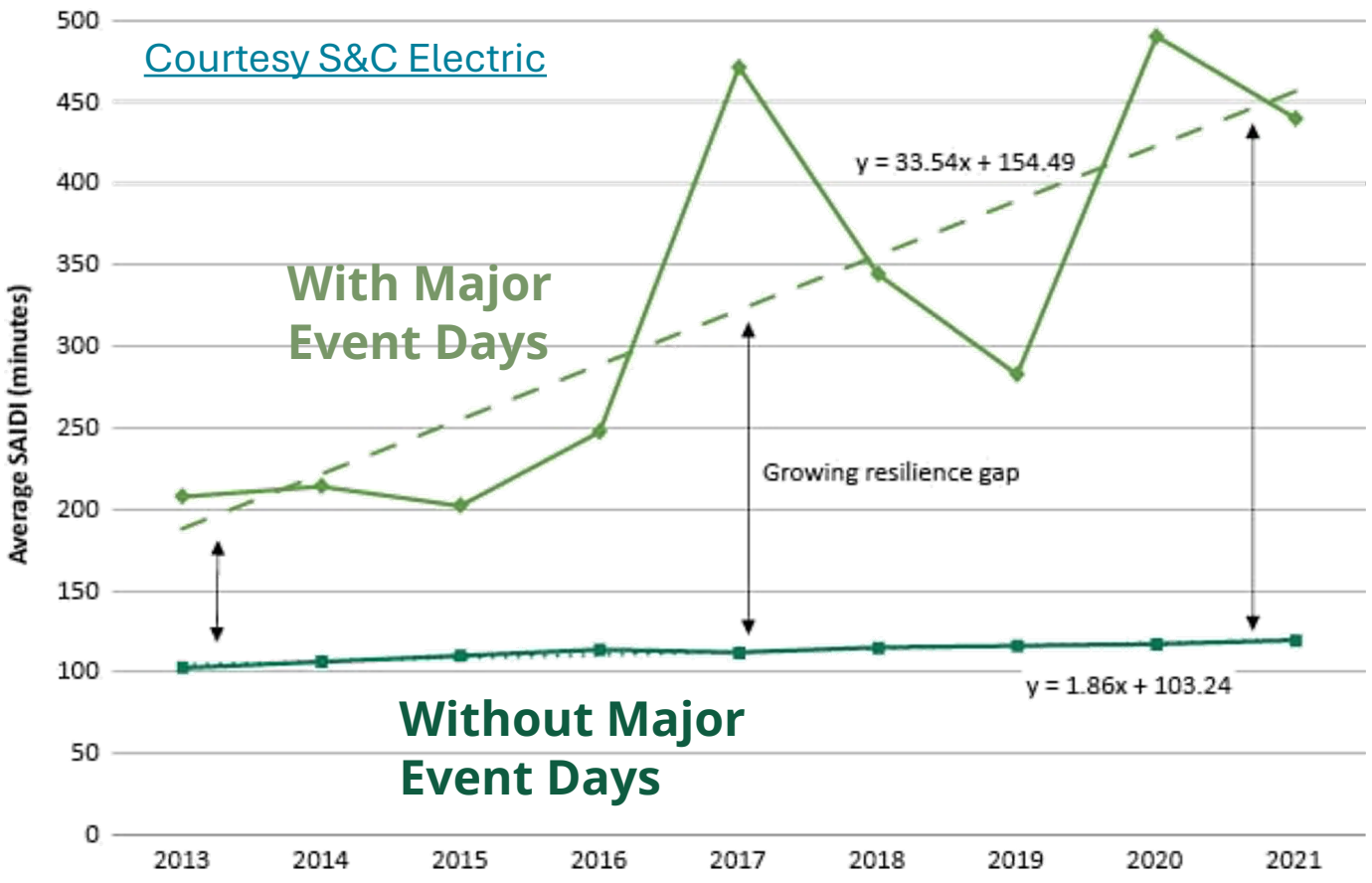
Texas Power Crisis (2021)
- 200-700 estimated fatalities
- >$195B damage
- Caused by cold

Hurricane Beryl (2024)
- 70 fatalities, >$6.8B damage
- Texans use Whataburger app to track outage because utility can't provide real-time info

Hurricane Maria (2017)
- 2,975 fatalities
- >$90B damage
- All of Puerto Rico (3.4M) without power
- Longest blackout in US history

PROJECT DETAILS

PROBLEM STATEMENT



Power Systems are showing an **increase in Harsh Environments** that they experience

- Natural Disasters
- Long-term Operating conditions

Resulting in **poorer power reliability** for customers

The Grid of the Future needs to be:

Highly agile

Multiply connected

Programmable (controllable)

Arbitrary Power and Reactive Power Control
Complete Nodal Control
Network of asynchronous coupled grids

Reconfigurable

SAIDI (System Average Interruption Duration Index)
metric for total average time a customer experiences a power outage over a year

PROJECT DETAILS

Power Electronics <u>are</u> the fundamental building block for the next generation grid

PROBLEM STATEMENT

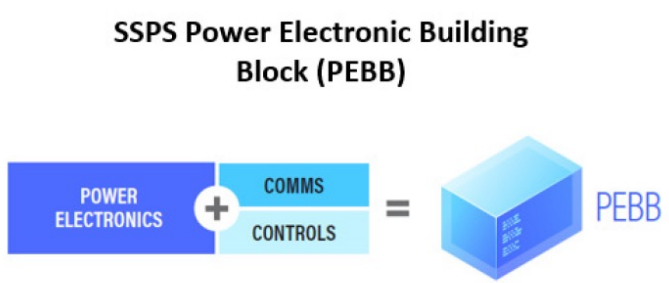
Power Infrastructure Today

Made-to-order, lead times of months or years
Monolithic – no soft failure
Logistically challenging, difficult to transport

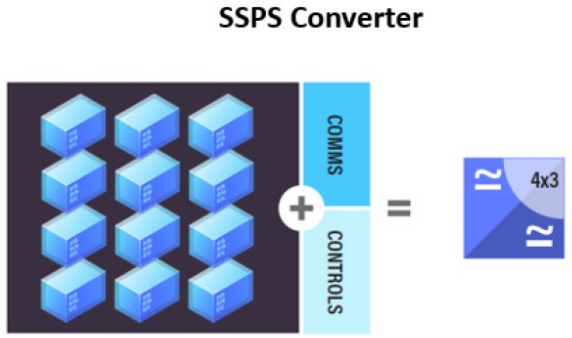
Power Infrastructure Tomorrow

Modular and fault tolerant
Agile, flexible, scalable, reconfigurable
Hot-swap replacement; simplified Operations and Maintenance





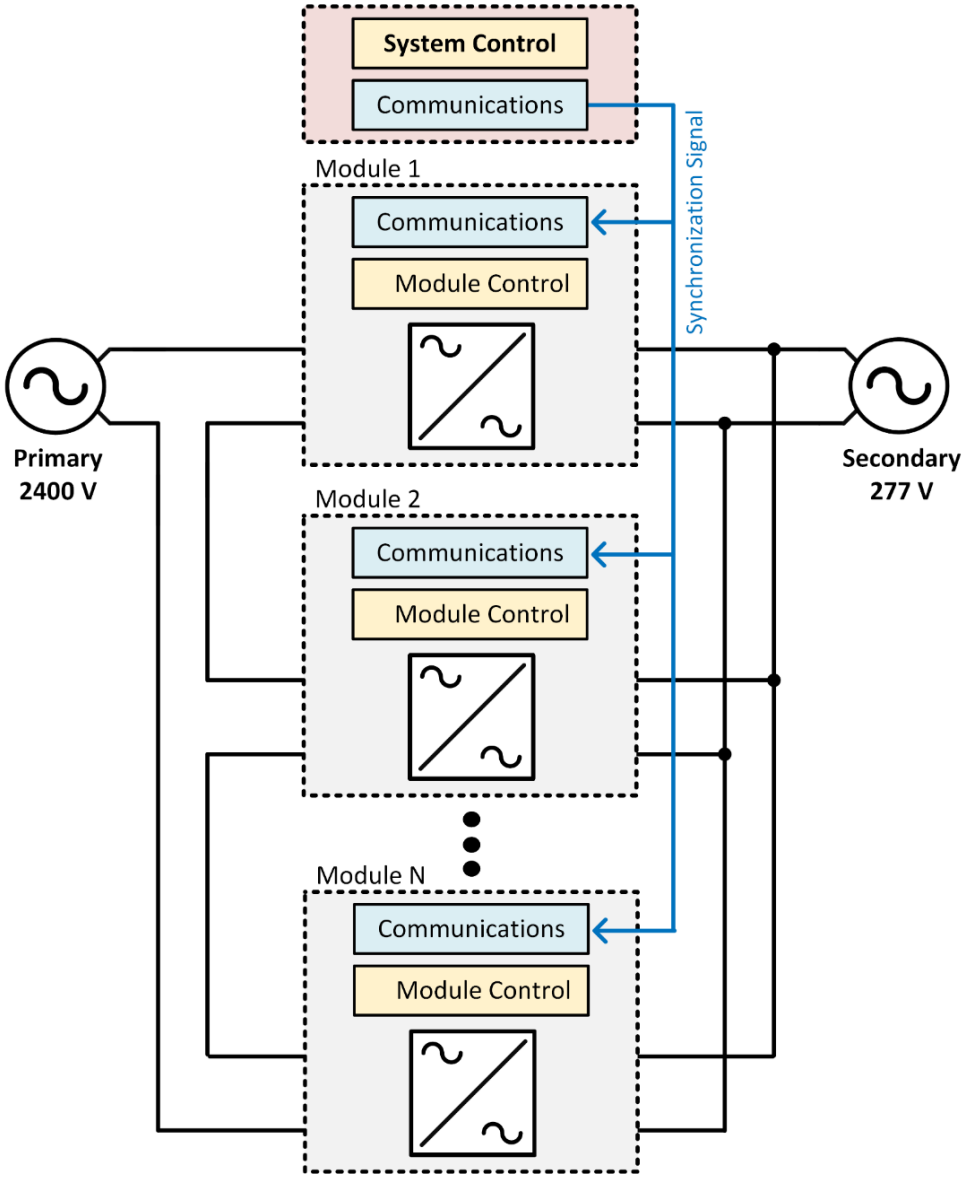






PROJECT DETAILS

TECHNICAL APPROACH/INNOVATION



Modular SSPS Structure

- Series connections at primary to scale voltage
- Parallel connections at secondary to scale current

Functionality (External View)

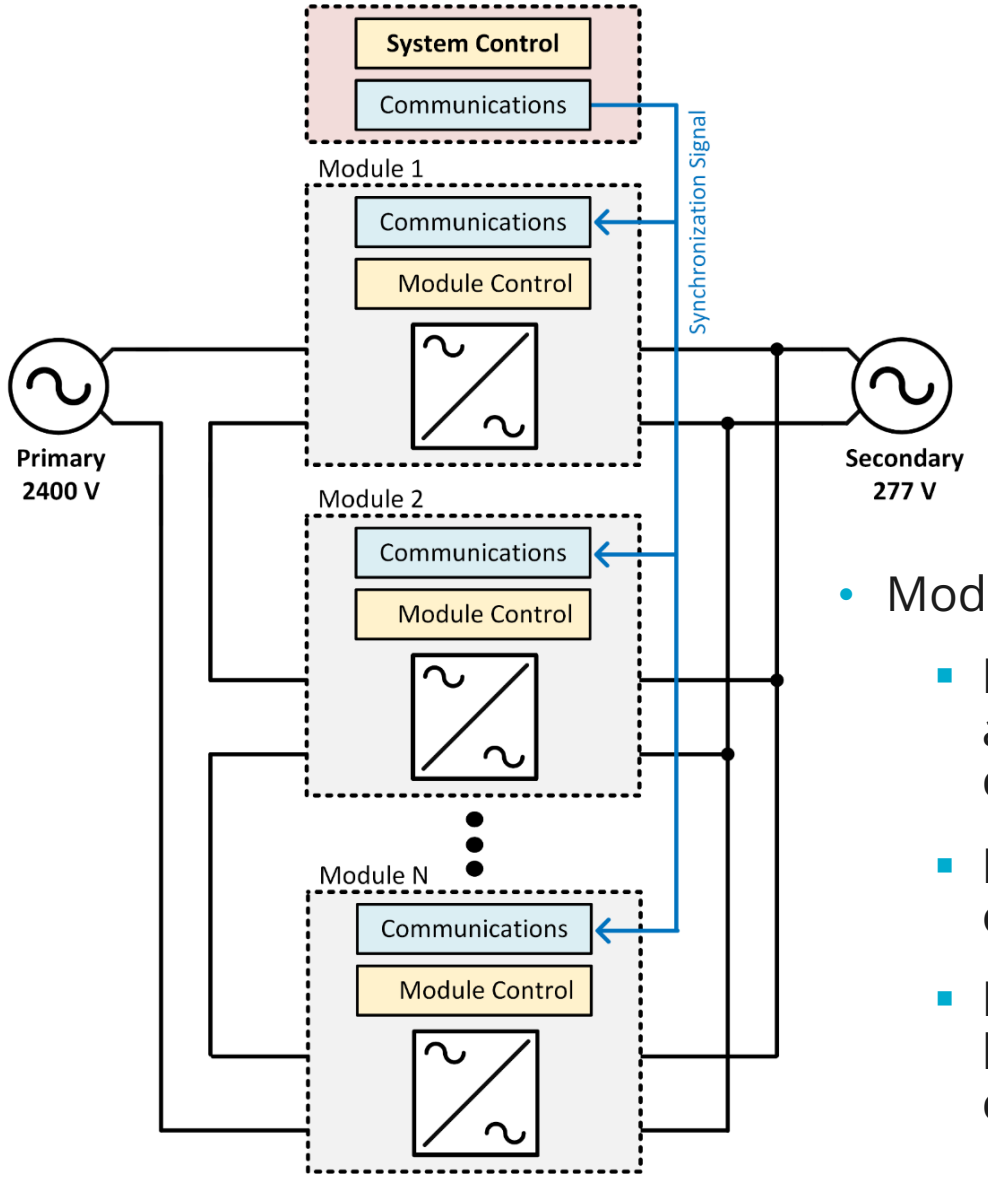
- Interconnect two grids with disparate voltage levels
- Galvanic isolation between primary and secondary
- Support multiple operational modes
  - Grid-forming operation (primary or secondary)
  - Arbitrary P/Q injection on operator command

Functionality (Internal View)

- Balance distribution of voltages at primary, currents at secondary
- Ensure each module operates within its own safe operating area
- Operate without high-bandwidth communications or strict synchronization

PROJECT DETAILS

TECHNICAL APPROACH/INNOVATION

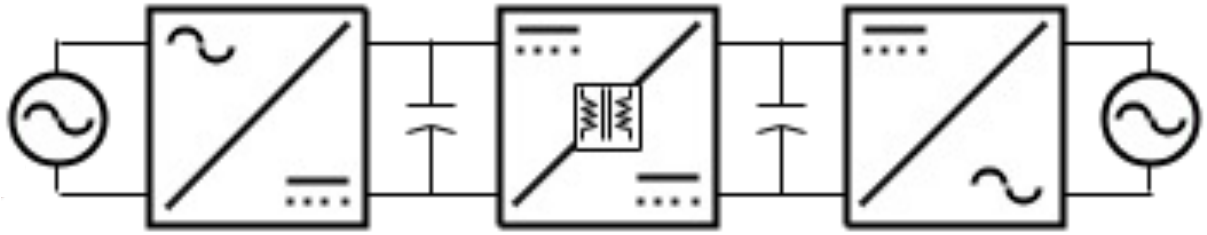




- Modular, flexible, and fault-tolerant solid-state power substations
  - **Modular**: Composed of standardized building block units which are highly transportable and easily integrated into complex power conversion assets
  - **Flexible**: General purpose building block units serve a broad range of end-use applications, power ratings, and voltage levels
  - **Fault-tolerant**: No single unit acts as single point of failure. System level operation is robust to internal faults and protected from cascading failure events.

PROJECT DETAILS

TECHNICAL APPROACH/INNOVATION

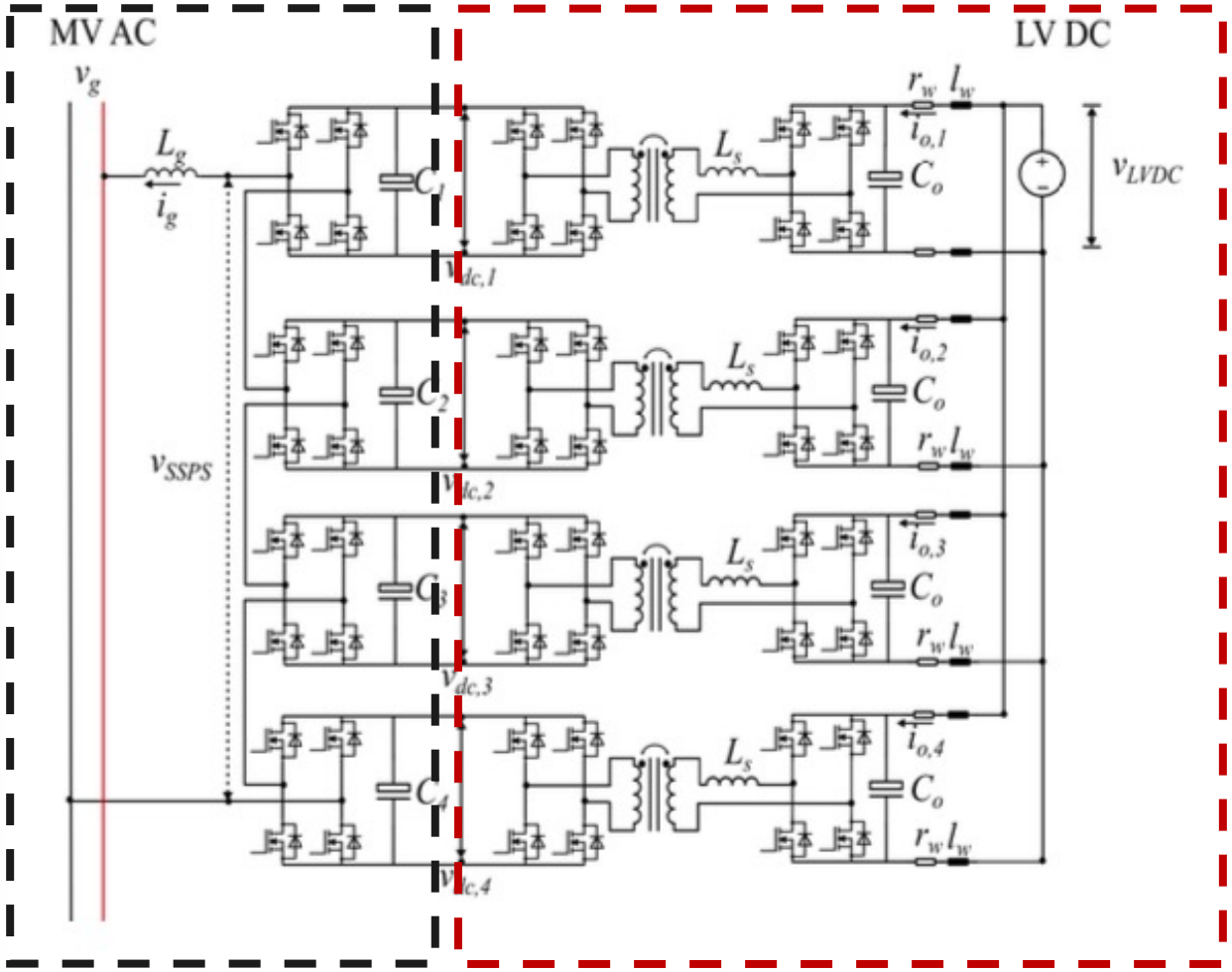


Multi-stage with low and high voltage DC link

Type IV SSPS

Active Front-End Cascaded H-bridge

Dual Active Bridge

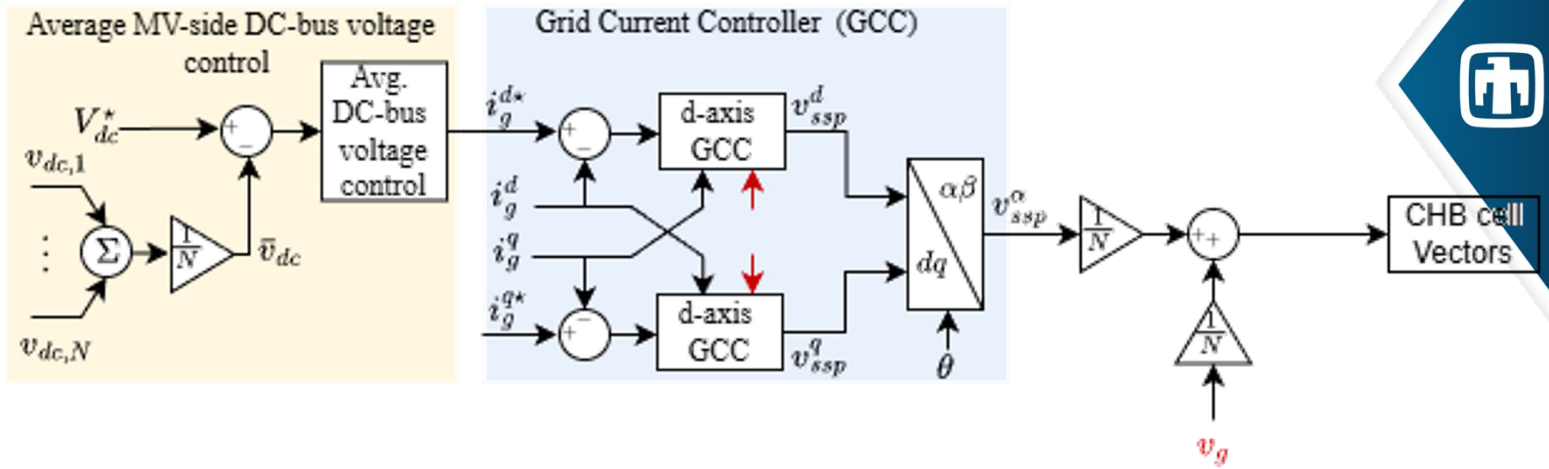


Parameter	Value
Interconnection voltage	4160 V (l-l), 60 Hz
Rated Power	60 kW
Number of cells per phase	4
Rated power per cell	15 kW
Output DC link Voltage	850 V
AFE DC link Voltage	1130 V

PROJECT DETAILS

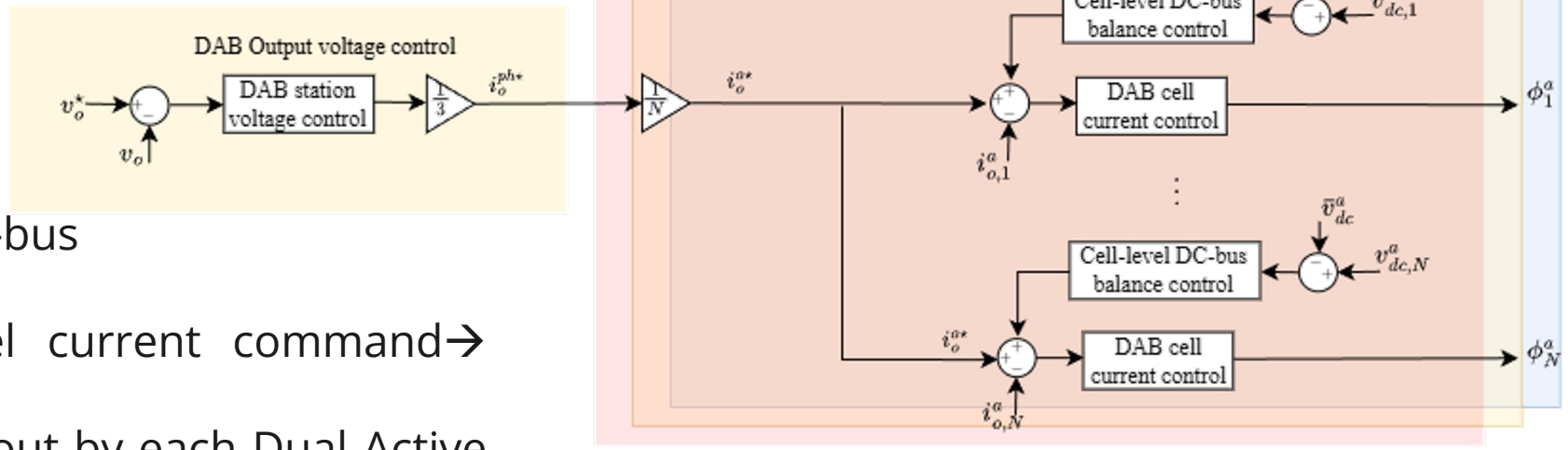
TECHNICAL APPROACH/INNOVATION

Cascaded H-bridge control



- **Control objective:** High Voltage DC-bus
- The grid voltage information usually fed forward into the dq current controller in rotating frame → Can limit the system response during fast transients, as converter produces incorrect voltage vectors
- V_{grid} directly fed forward in stationary frame –> Response time loop (PLL) bandwidth and limited only by voltage-sensing delays

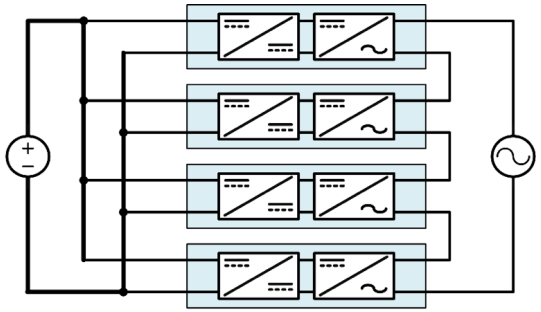
DAB control



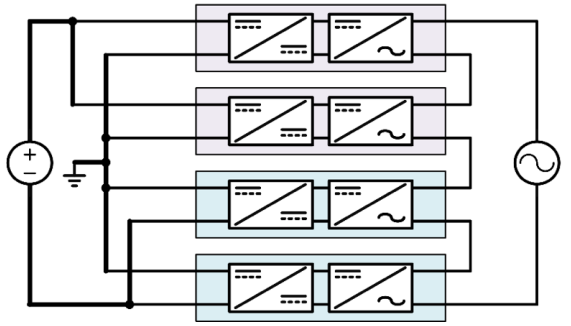
- **Control objective:** Low Voltage DC-bus
- Dual-loop strategy
- Outer loop generates station-level current command→ each cell of the SSPS.
- Cell-level voltage balancing carried out by each Dual Active Bridge by adjusting current command at cell level

PROJECT DETAILS

TECHNICAL APPROACH/INNOVATION

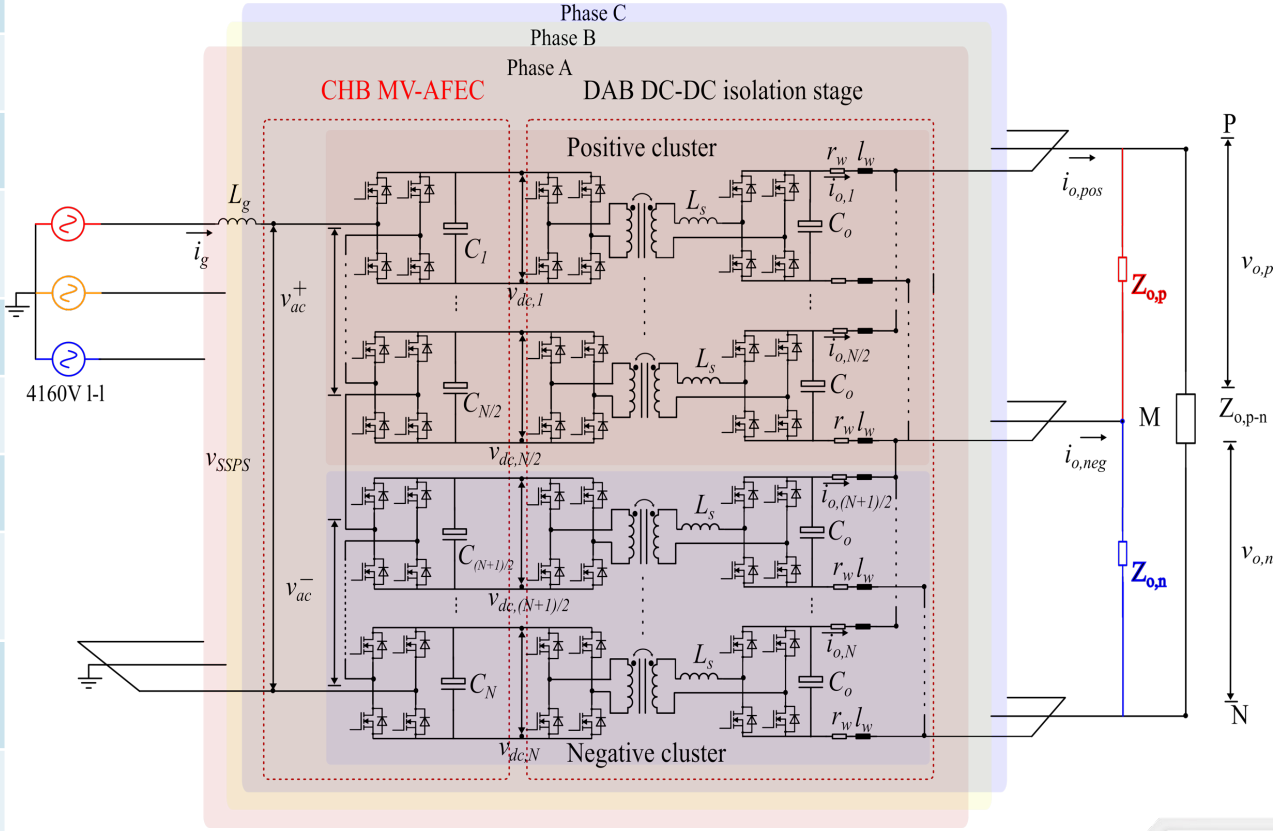


CONFIG 1 - UNIPOLAR



CONFIG 2 - BIPOLAR

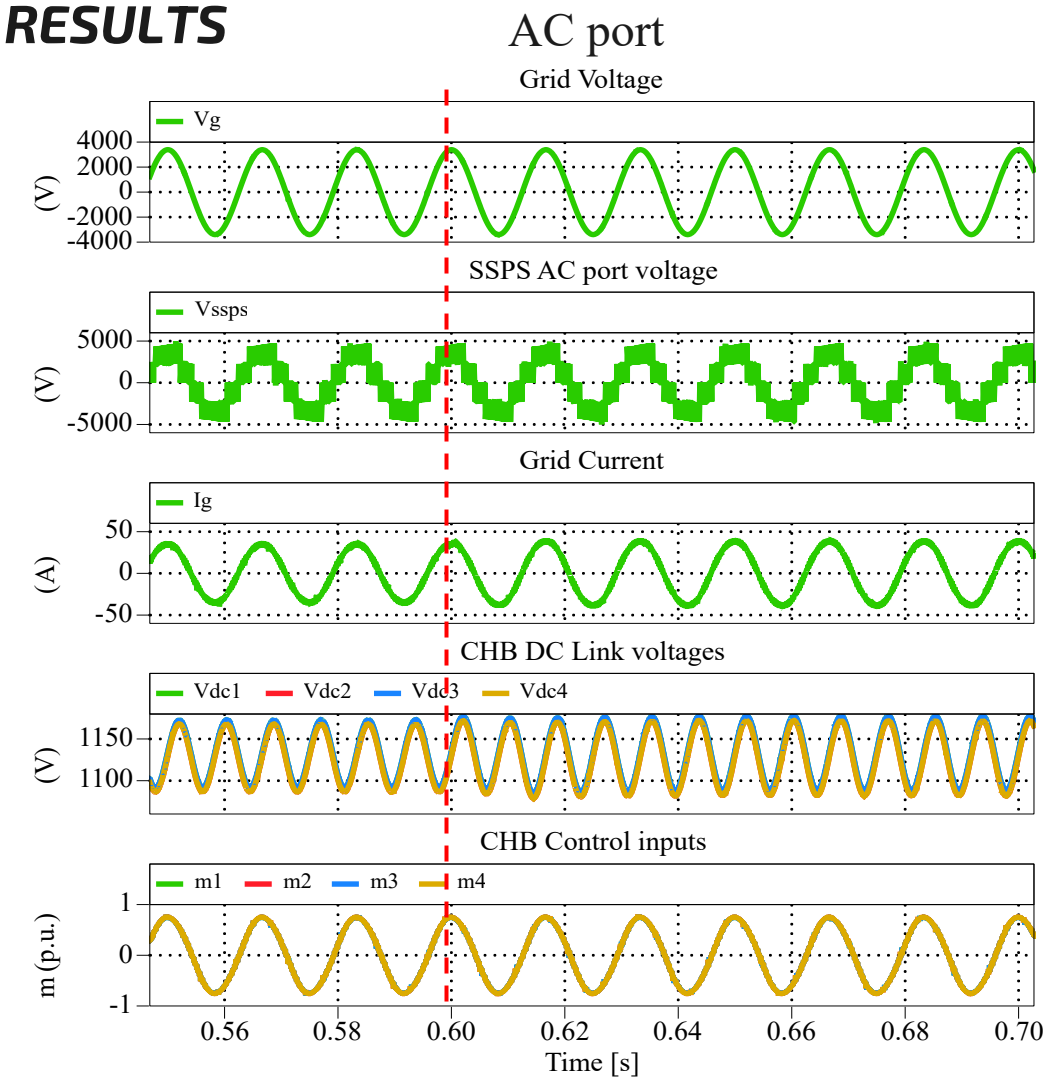
System Config.	AC phases	Brief description	Timeline
Config 1	1	Open Loop	11.18.2025
Config 1	1	Closed Loop	12.02.2025
Config 1	1	Dynamic load transients	12.16.2025
Config 1	1	Compliance to grid codes (Harmonics/LVRT)	01.27.2026
Config 1	3	Closed-loop, 3-phase SSPS	02.24.2026
Config 1	3	Dynamic operation, 3-phase	03.10.2026
Config 2	1	Bipolar DC bus	05.05.2026
Config 2	1	Dynamic operation with split bus	06.30.2026
Config 2	3	3-phase with a split bus	08.11.2026
Config 2	3	Dynamic operation with split bus	09.30.2026

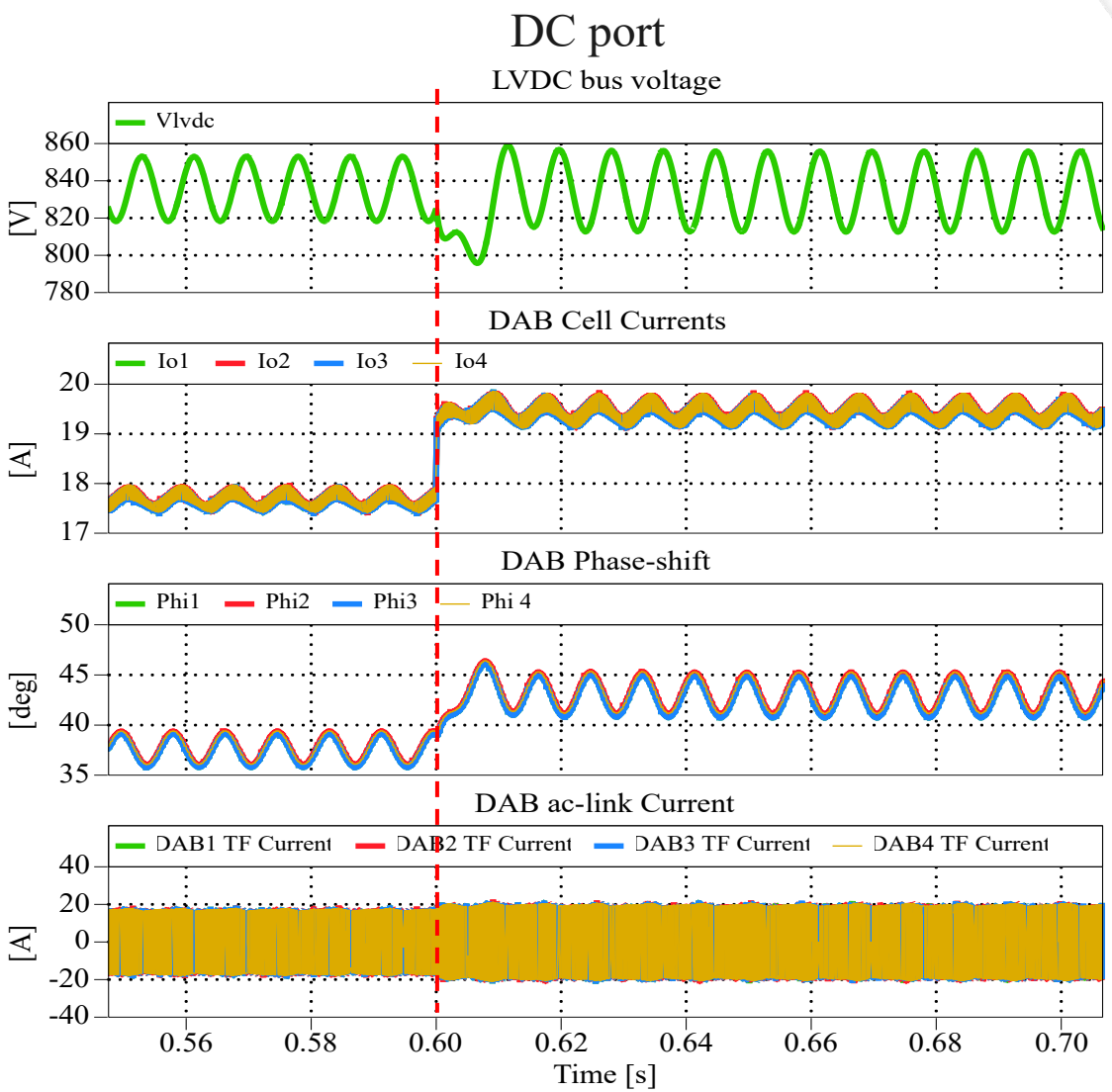


PROJECT DETAILS

DYNAMIC SIMULATIONS

RESULTS





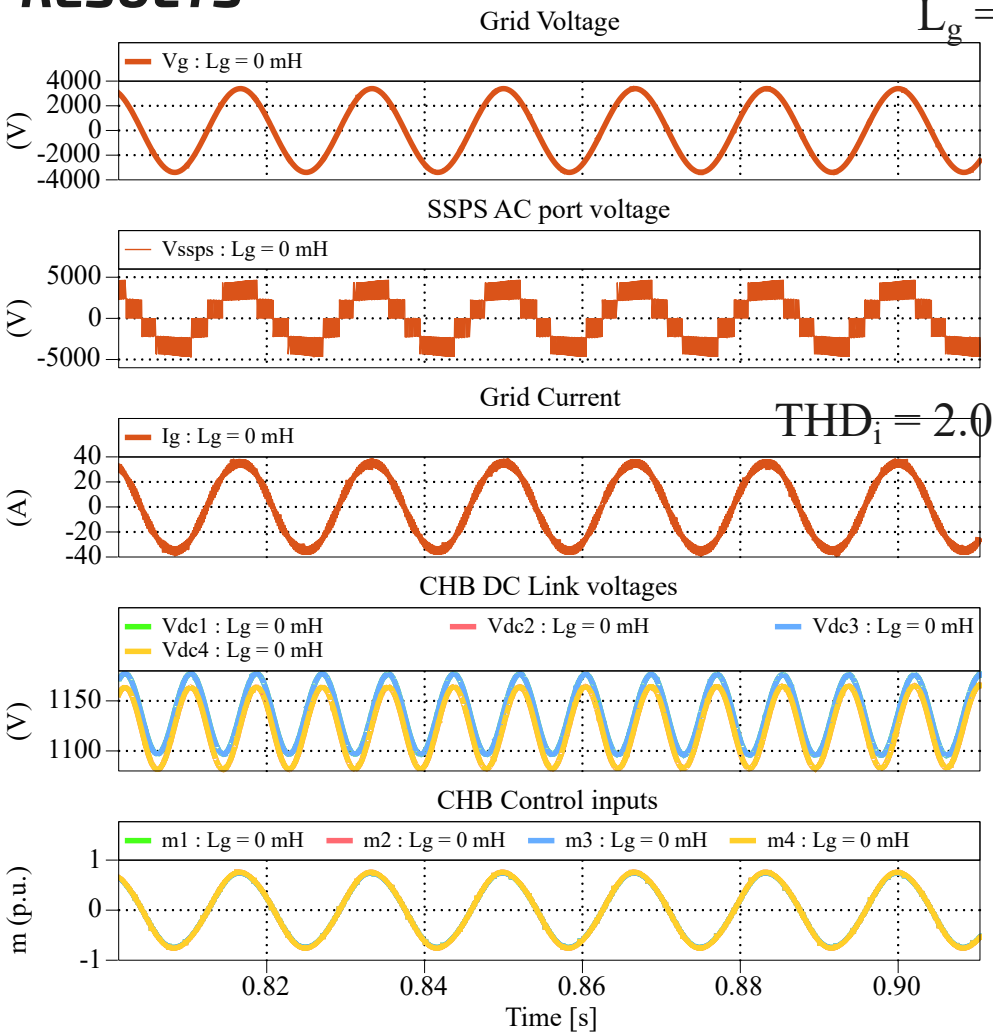
- At time t = 0.6s, the load power is increased by 10%.
- The CHB MV-side DC link remains well regulated throughout due to load power feed-forward to the CHB current controller

PROJECT DETAILS

MEDIUM VOLTAGE AC PORT – EFFECT OF GRID IMPEDANCE

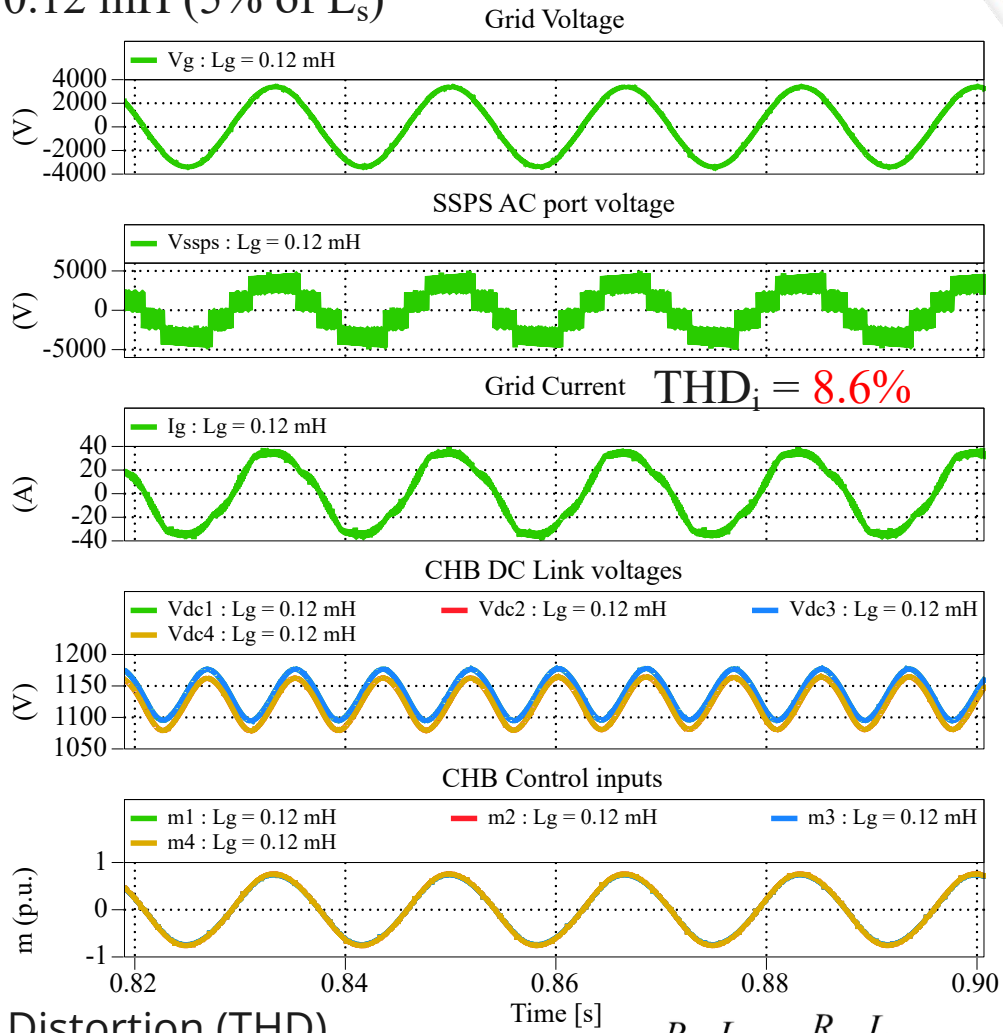
RESULTS

$L_g = 0$



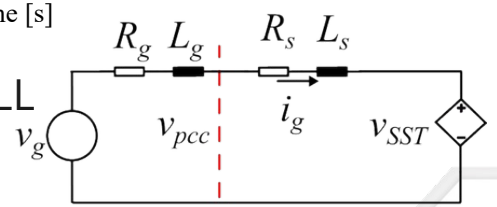
$THD_i = 2.09\%$

$L_g = 0.12$ mH (5% of L_s)



$THD_i = 8.6\%$

- Presence of grid impedance deteriorates the current Total Harmonic Distortion (THD)
- Presence of switching ripple in sensed point of common coupling voltage adversely affects the PLL
- Requires oversampling of point of common coupling voltage waveform to correct back to 2%



PROJECT DETAILS

RESULTS

IEEE 1547-2022 (LVRT/HVRT)

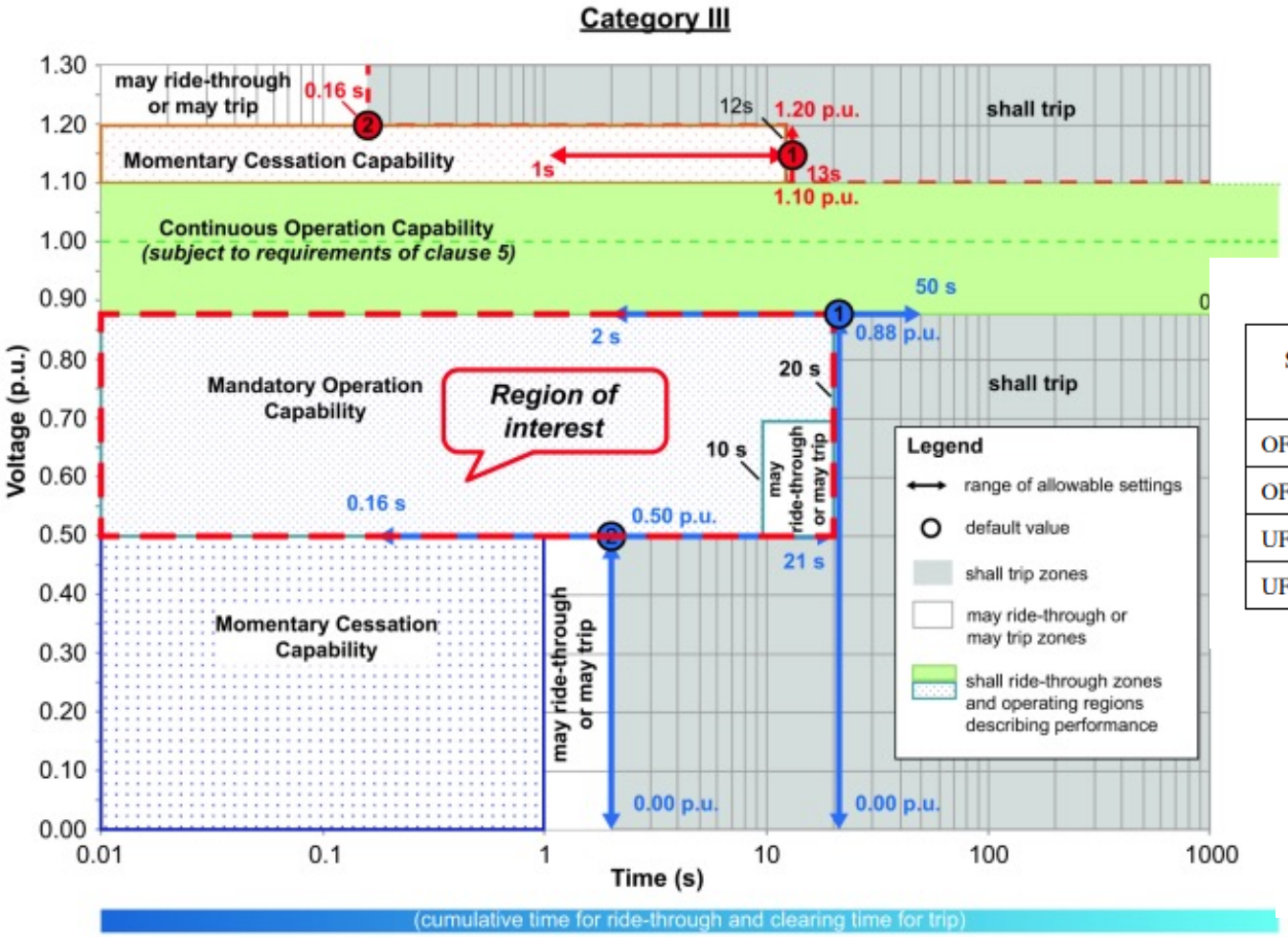


Figure 37—Dynamic Voltage Support Function – Applicable Regions of Interest

Table 10—Frequency trip settings

Shall trip function	Default settings		Ranges of allowable settings	
	Frequency (Hz)	Clearing time (s)	Frequency (Hz)	Clearing time (s)
OF2	62.0	0.16	61.8–66.0	0.16–1000.0
OF1	61.2	300	61.0–66.0	180.0–1000.0
UF1	58.5	300	50.0–59.0	180.0–1000.0
UF2	56.5	0.16	50.0–57.0	0.16–1000.0

Table 11—ROCOF ride-through requirements

Category I	Category II	Category III
0.5 Hz/s	2.0 Hz/s	3.0 Hz/s

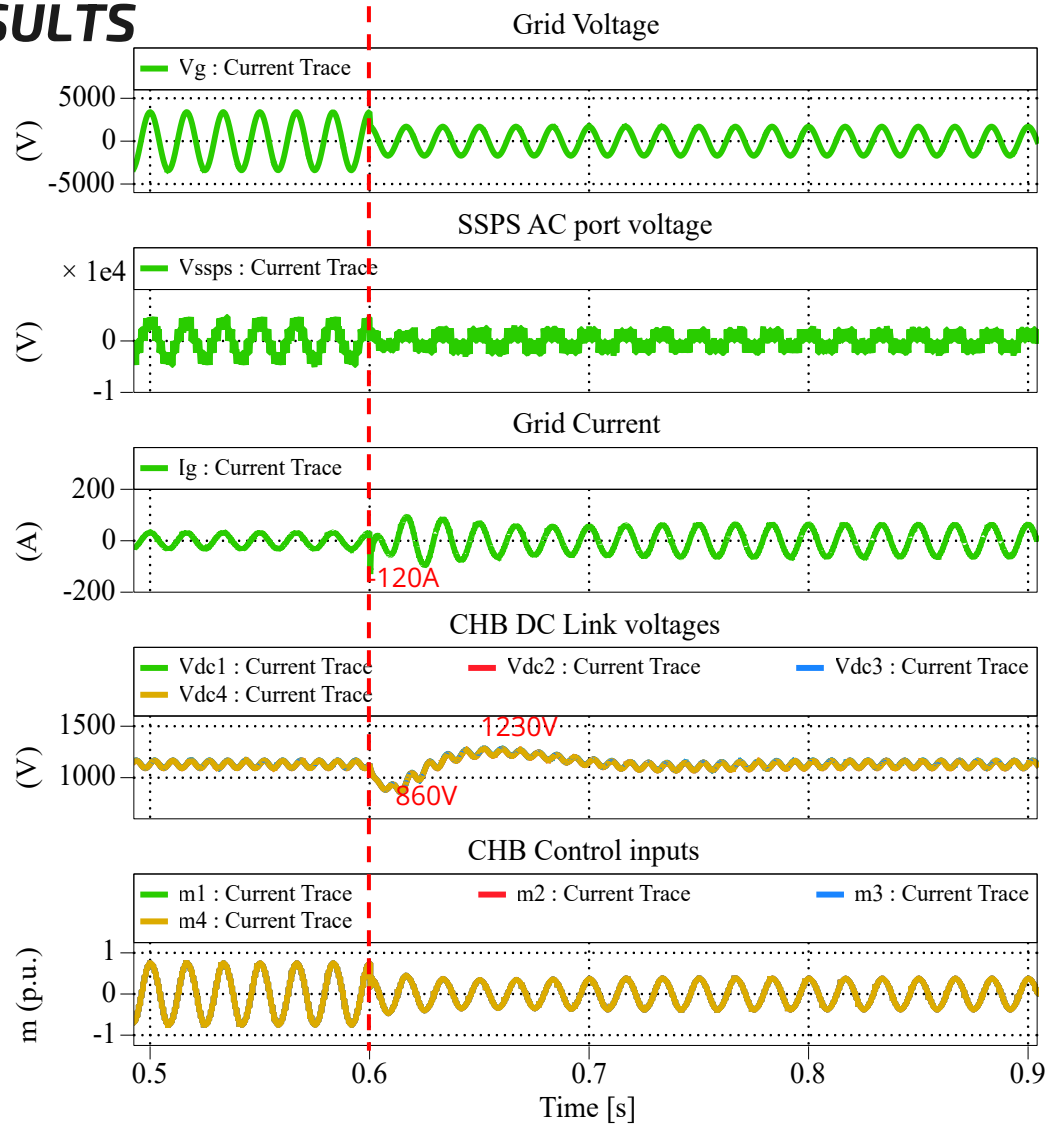
Source: Table 21 of IEEE Std 1547-2018

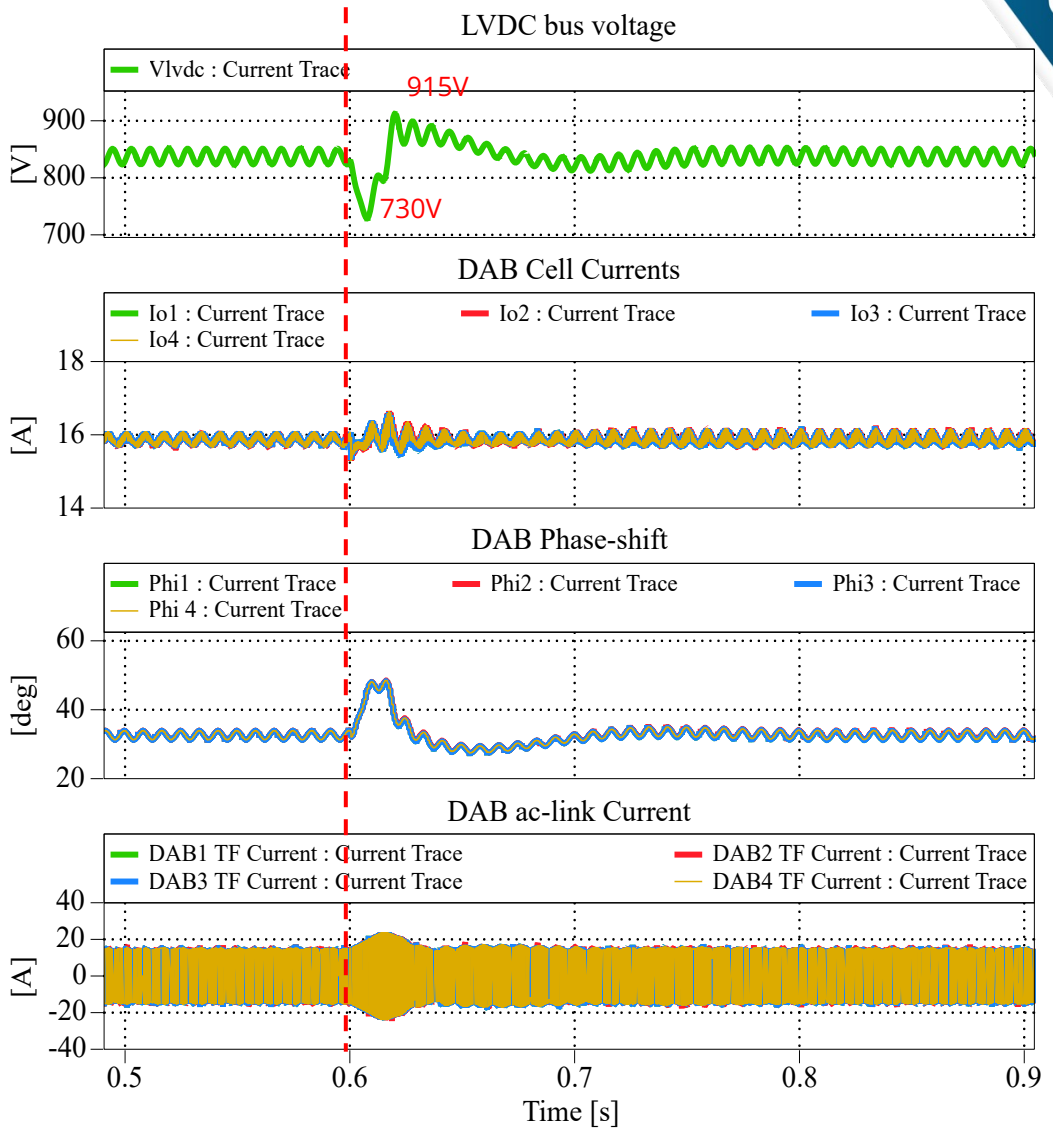
- Interest from controls perspective: Ensure designed controls are adequate to mitigate transients
- Simulations conducted at 0.5 and 1.2 p.u. respectively.

PROJECT DETAILS

RESULTS

LVRT OPERATION





- Results in voltage deviation on HV and LV DC bus. Must increase grid current controller bandwidth 500 Hz to 1 kHz (Control rate: 10 kHz) to mitigate transient
- Large initial spike in current due to the selected filter inductance value

PROJECT DETAILS

RESULTS

- Developing Documentation
  - Specification sheet
  - Manual
  - Interface Description
- Identify gaps in knowledge
- ***Identify requirements for testing***

Standard	Use Case
IEEE P2800	Transmission Connected Generation
IEEE 1547	Distribution Connected Generation
IEEE 1378	HVDC Stations
IEEE 1709	Shipboard MVDC
IEEE 2892	MVDC "Transformers"
MIL-STD-1399-300-3	Shipboard MVDC
IEC 63604 (DRAFT)	Power Electronic Transformers

RELEVANT STANDARDS EVALUATION

Characteristics	Requirement
Frequency	
(a) Nominal frequency	60Hz
(b) Frequency tolerance	+/- 3%
(c) Frequency modulation	0.5 %
(d) Frequency transient	
(1) Tolerance	+/- 4%
(2) Recovery time	2 seconds
(e) The worst-case frequency excursion from nominal frequency resulting from (b), (c) and (d)(1) combined under emergency conditions	+/- 5.5%
Voltage:	
(f) Nominal user voltage	4,160; 6,600; 13,800 Vrms

Ship MVAC Interface

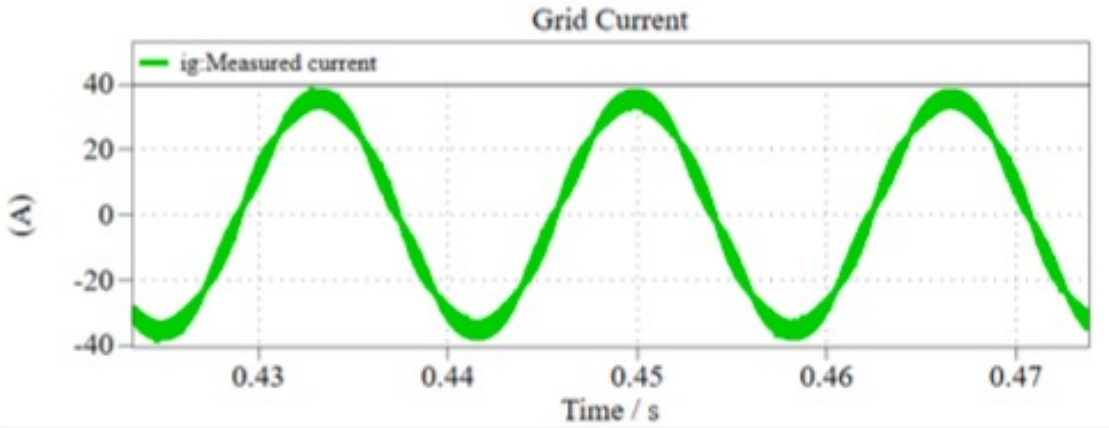
Draft Specification Sheet

Electrical Power	
Input Power	
Maximum Available Input Power	TBD PU
Input Voltage	LN of 4160 per LRU, 15 kV rms (multiple LRU), 3-phase
Input Frequency	60 Hz
Output Power	
Output Voltage	+/- 850 V DC
Details	Two power DC outputs: + 850 V DC and – 850 V DC nominal to common One common: 0 V DC
Tolerance	+/- 10%
Range	over the operational envelope from no load to full load
Output Current	42 A DC per LRU at maximum power ratings
Details	60 amps is the maximum current drawn under a "low-line" condition, when the output voltage is +/- 765 V DC.

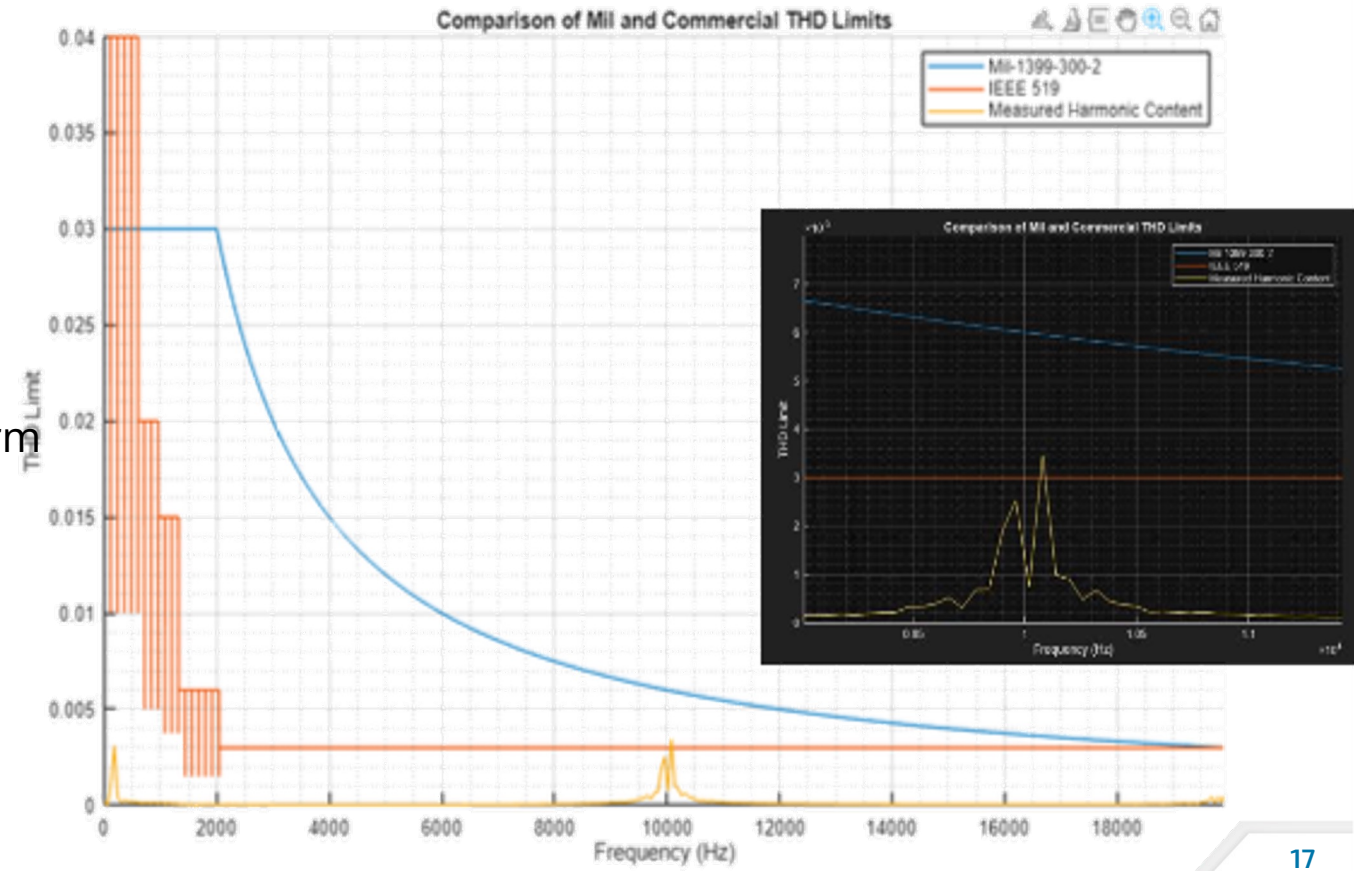
PROJECT DETAILS

AUTOMATED ANALYSIS FOR STANDARDS APPLICABILITY

RESULTS



Simulated or Experimental Waveforms



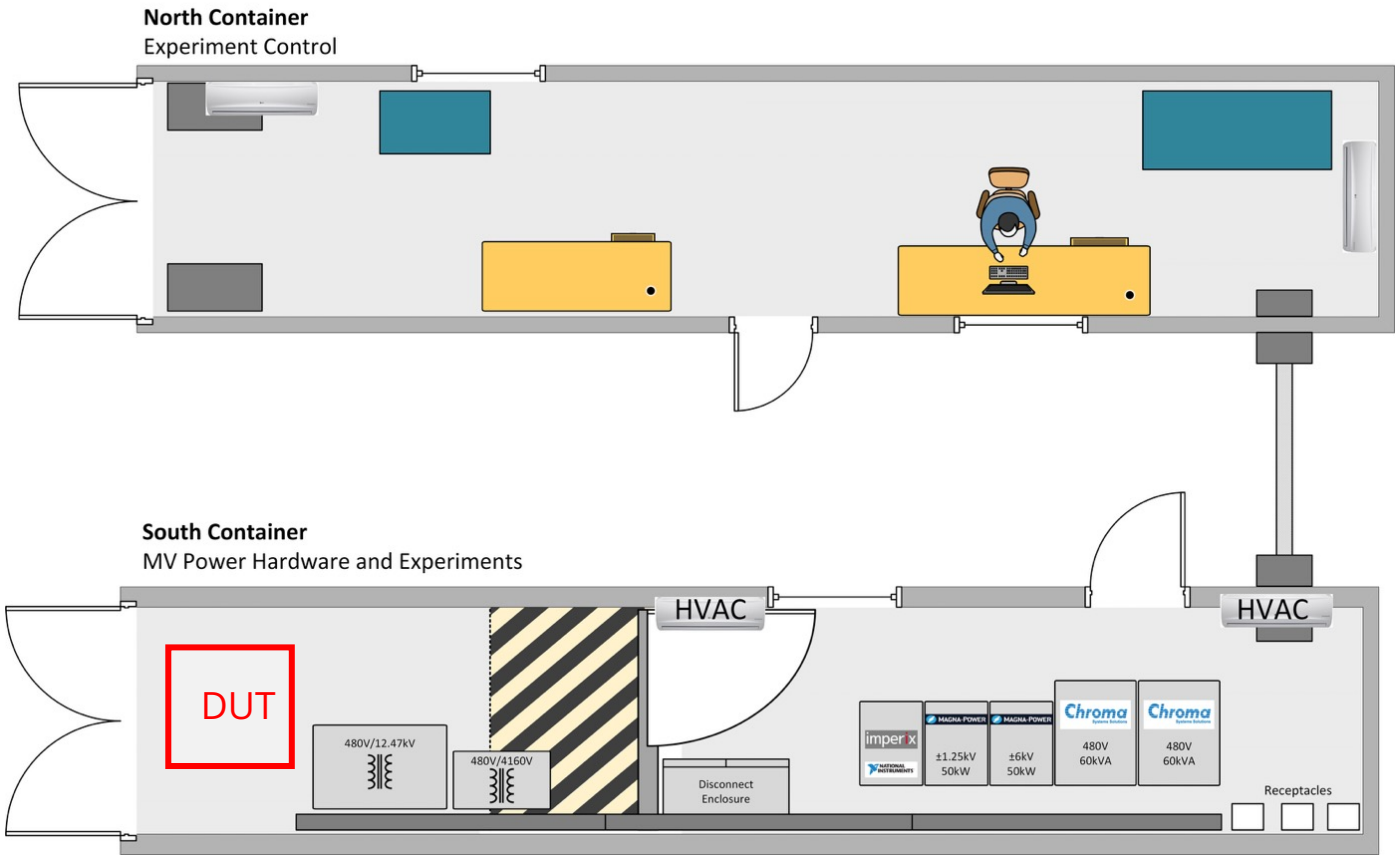
- Developed scripts to automatically check compliance of time series data to relevant standards
  - Simulated or experimental waveforms
- Example of THD compared to MIL-1300 and IEEE 519
- Developed scripts for voltage, power, frequency, waveform quality
  - THD
  - Transient behavior
  - Excursions from allowable tolerances
  - Pulsed power limits

PROJECT DETAILS

MEDIUM VOLTAGE EXPERIMENTAL TESTING (YEAR 2)

COMMISSIONED 2025

RESULTS







Power Electronics Evaluation up to:

- 60 kVA (more in loopback configuration)
- 12.47 kVac (35 kVac in progress)
- 12 kVdc
- 30 kA AC fault current (in progress)
- 10 kA DC fault current (in progress)

PROJECT DETAILS

RESULTS

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TESTING PROTOCOLS

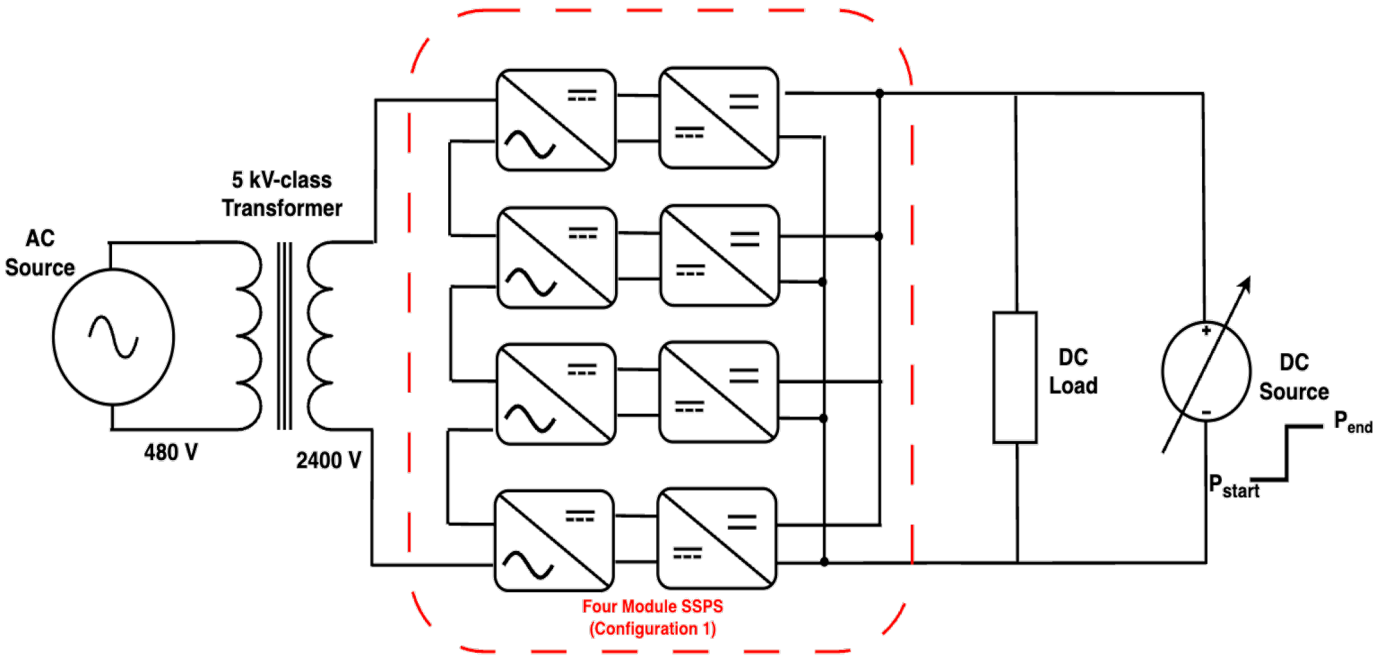
- Developing full testing protocols for evaluation of SSPS in year 2 of project
- Functional Testing
  - Unit powers up correctly, enters intended control modes, responds predictably
  - Ensures safe operation
  - Open Loop and steady state operation
- Dynamic Testing
  - Command steps, load changes, and source disturbances
  - Closed-loop operation beyond steady-state
  - Verify control modes remain stable during rapid changes, transitions occur predictably, and that the SSPS does not nuisance trip
- Contingency Testing
  - Behavior under abnormal, but credible conditions
  - Confirm system responds in a controlled, safe, and useful manner
  - Includes module bypass (input and output)

PROJECT DETAILS

TESTING PROTOCOLS

- All tests have:
  - Diagrams and Equipment List
  - Full parameters for Testing
  - Data acquisition collection and analysis requirements
  - ***Does not*** include pass/fail metrics

RESULTS



Bidirectional Power Flow Testing

Quantity	Parameter	AC/DC-side
Rise/Fall time to 90/10%	$I^{sys}_{in/out}$ or $V^{sys}_{in/out}$	Both
Over/undershoot peak	$I^{sys}_{in/out}$ or $V^{sys}_{in/out}$	Both
Settle time to ±5%	$I^{sys}_{in/out}$ or $V^{sys}_{in/out}$	Both
N^{th} Module Voltage Balancing	$V^{mod,N}_{in}$/ V^{sys}_{in}	AC
N^{th} Module Current Balancing	$I^{mod,N}_{out}$/ I^{sys}_{out}	DC
Oscillation frequency	$I^{sys}_{in/out}$ or $V^{sys}_{in/out}$	Both

Test #	AC Input Voltage	AC Source PF	Start DC Load Power (p.u.)	Final DC Load Power (p.u.)
1	2400	1	0	-0.5
2	2400	1	0	-1
3	2400	1	-0.5	-1
4	2400	1	-0.5	0
5	2400	1	-0.5	0.5
6	2400	1	-1	1
7	2400	0.9 Leading	0	-0.5
8	2400	0.9 Leading	0	-1
9	2400	0.9 Leading	-0.5	-1
10	2400	0.9 Leading	-0.5	0
11	2400	0.9 Leading	-0.5	0.5
12	2400	0.9 Leading	-1	1
13	2400	0.9 Lagging	0	-0.5
14	2400	0.9 Lagging	0	-1
15	2400	0.9 Lagging	-0.5	-1
16	2400	0.9 Lagging	-0.5	0
17	2400	0.9 Lagging	-0.5	0.5
18	2400	0.9 Lagging	-1	1

PROJECT DETAILS

CONCLUSION & IMPACT

- Developed controls for ***modular, 5kV-class SSPS***
- Detailed simulations under variety of ***normal and contingency conditions***
  - Two configurations (unipolar and bipolar)
  - Single and three-phase systems
  - Open-loop, closed-loop, and dynamic simulations
  - Evaluation of operation during contingency conditions
    - LVRT
    - Unbalance loads (DC/AC)
    - Grid impedance
- Evaluated applicable standards landscape for SSPS
  - Automated testing scripts to evaluate standards compliance
- Developed Testing protocol for medium voltage SSPS
  - Informed by relevant standards landscape
  - Normal and contingency operating conditions
  - Aligns future testing with simulations
- Year 2 will focus on building and experimentally validating SSPS at 5 kV

Development of a high performance, manufacturable SSPS that aligns with the current standards landscape will enable the next generation grid that is agile, robust, and cost-effective

PROJECT DETAILS

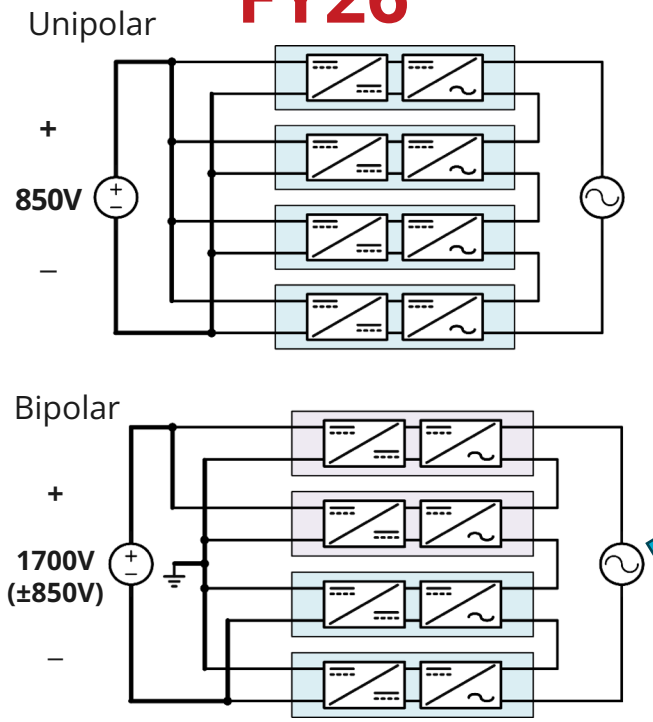
FUTURE DIRECTION/NEXT STEPS

Develop and validate controls for fault tolerance

Demonstrate practical capabilities of the building block framework

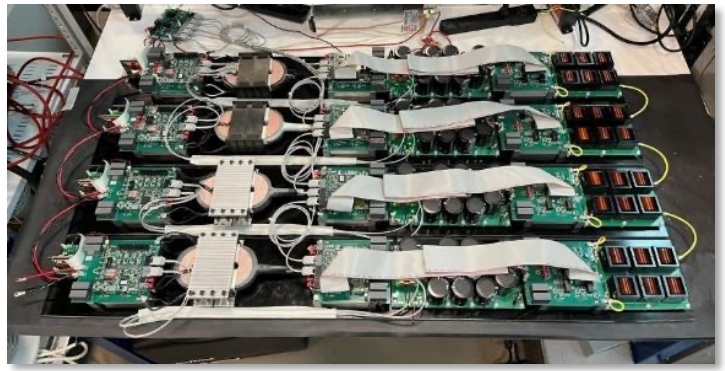
De-risk deployment and commercialization of Medium Voltage SSPS technologies

FY26



Simulate

FY27



Build



Test



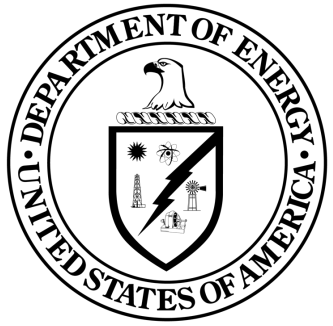
03/31/2027: Fabrication of one Y-leg of a 4160V grid tied SSPS

09/30/2027: Experimental results for evaluation of two SSPS topologies

09/30/2027: Scale-up and manufacturability plan for sub-modules and systems

ACKNOWLEDGEMENTS

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U.S. DEPARTMENT of ENERGY

THANKS FOR YOUR ATTENTION



Participants from the Power Electronics Workshop held in Albuquerque New Mexico in August of 2025

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