Advanced Submodule Designs for Cost-Effective and Miniaturized High-Performance Data Center Converters (ASCEND-DC)

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DOE OE TRAC Peer Review 2026

Topic Area: Component Design and Development

Topic Area Objective - R&D that supports reducing converter station costs by 35% by 2035 in accordance with DOE's COst REduction (CORE) initiative

Project Description:

- National Laboratory of Rockies (NLR), in collaboration with Arizona State university (ASU) and Oak Ridge National Laboratory (ORNL), is developing **innovative submodule (SM) designs** for low-cost converters.
- **Objective:** Miniaturize modular multilevel converters (MMCs) to reduce converter station costs.
- The project will lead to **prototype development** of submodules and miniaturized MMCs.
- NLR will leverage the **ARIES platform** to validate innovations at bulk transmission scale.
- An **Industry Advisory Board (IAB)** will provide project guidance, with contributions from:
  - **Wolfspeed Inc.,** is an American company designs and manufactures silicon carbide technology, is also supporting HVD SM development.
- **TRL Start: 2**
- **TRL End: 6**

Prime National Lab(s):

National Renewable Energy Laboratory

Principal Investigator(s):

Yashodhan Agalgaonkar (NLR)

Major Team Participants:

Sreenivasa S. Jaldanki (ORNL)

Mike Ranjram, Raja Ayyanar, Vijay Vittal (ASU)

Industrial Advisory Board:

Wolfspeed Inc.,

Mitsubishi Electric Power Products, Inc. (MEPPI),

National Centre, UK

Funding Profile : $1.2M

NREL (508K), ORNL (304K), ASU (388K)

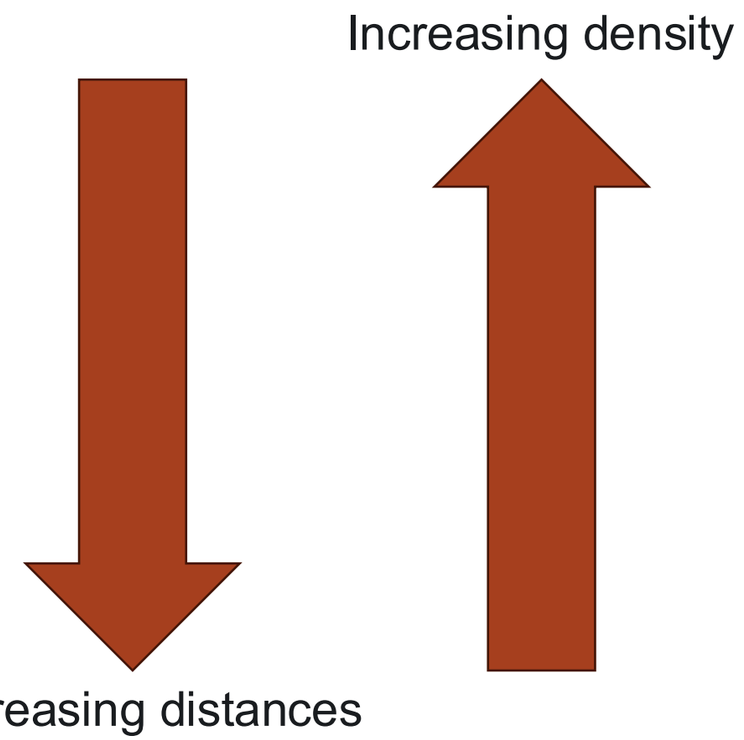
Period of Performance: 2 Years

Power Distribution Architectures for Hyperscale Data centers

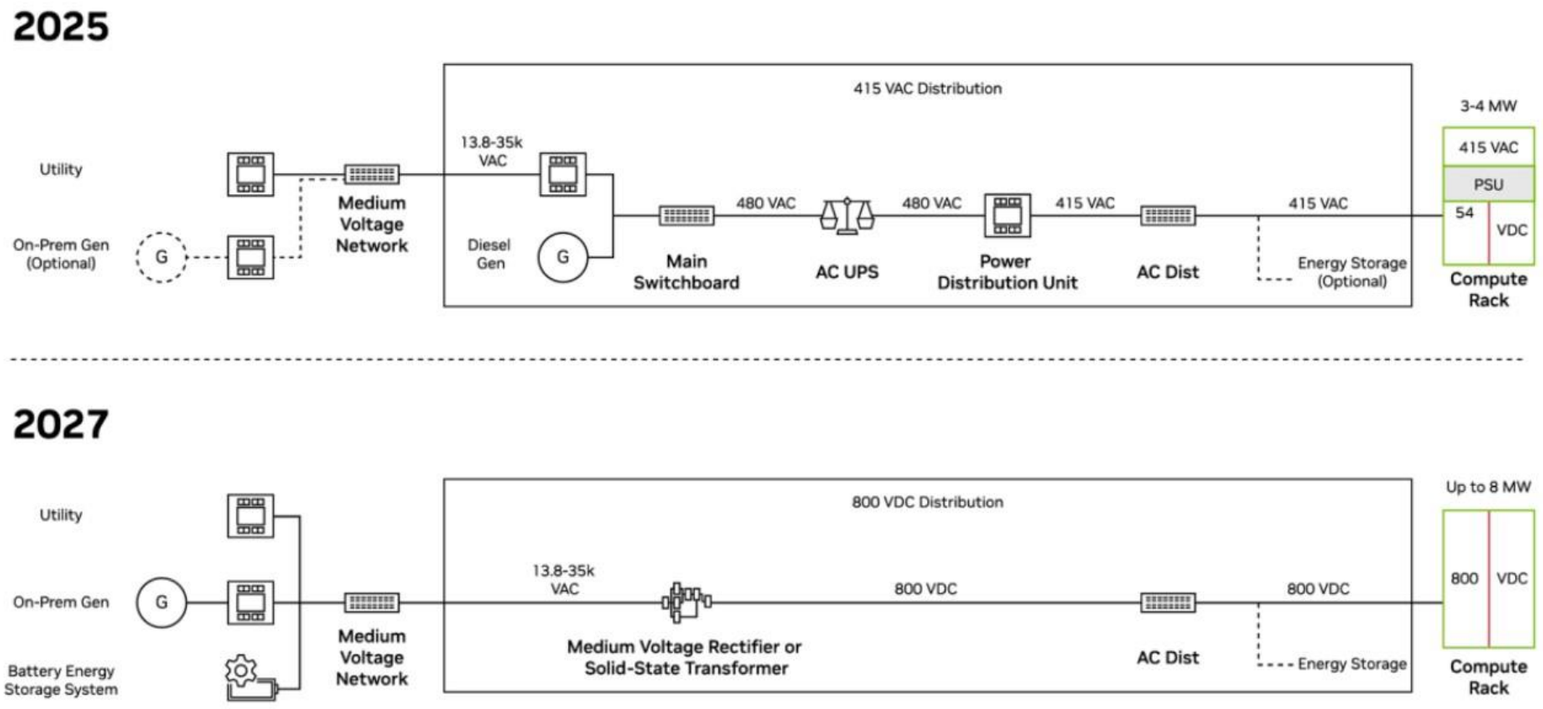
- Understanding physical layout is required to intelligently investigate new power distribution concepts
- Catalogued the upcoming Data centers into three categories:

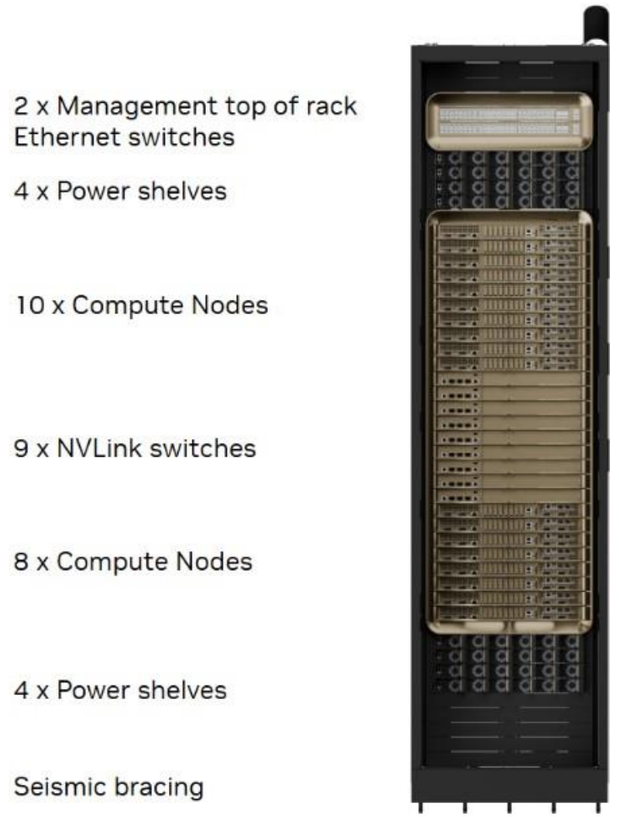
  - **Monoliths [1]:** 1-2 buildings at about 1-2 million sq. ft on approximately 100 acres, Developed by xAI
  - **Campuses [2]:** 8-30 buildings co-located over 1-2 miles and approximately 1000 acres, Developed by Amazon
  - **Clusters [3]**: Local but not co-located campuses that can split the training workload; distributed over 15-50 miles and approximately 300 sq. miles, Develop by Google

- These confirm the importance and relevance of **medium voltage** distribution, which our project supports.



Evolution to 800V Data Center Distribution [4]

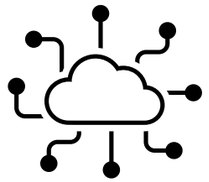




- Rack power levels are increasing dramatically – MW-scale racks expected by 2027.
- Data Centers ‘upgrading’ to **dc** distribution within the building to accommodate these powers
  - 800V distribution permits 157% more power in the same wire gauge as in 415Vac
  - DC aligns with dc nature of the load, removes redundant ac/dc conversions and can simplify battery backups (UPS)

Data Centers Have Historically Been a “Follower” Technology

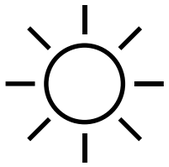
- Rack power levels have driven a massive shift to DC distribution within the data center
- Data Centers have been a “follower” technology
  - Shift from 12→48V benefits from expense of Telecom growing pains
  - Shift from 48 → ± 400V benefits from expense of EV growing pains
  - Natural next step is 1200/1500V distribution that has been commoditized by grid-tied solar PV
  - **<u>No next natural technology to adopt ⇒ Immense opportunity and need for power R&D</u>**



48V



400-900V



1.2-1.5kV



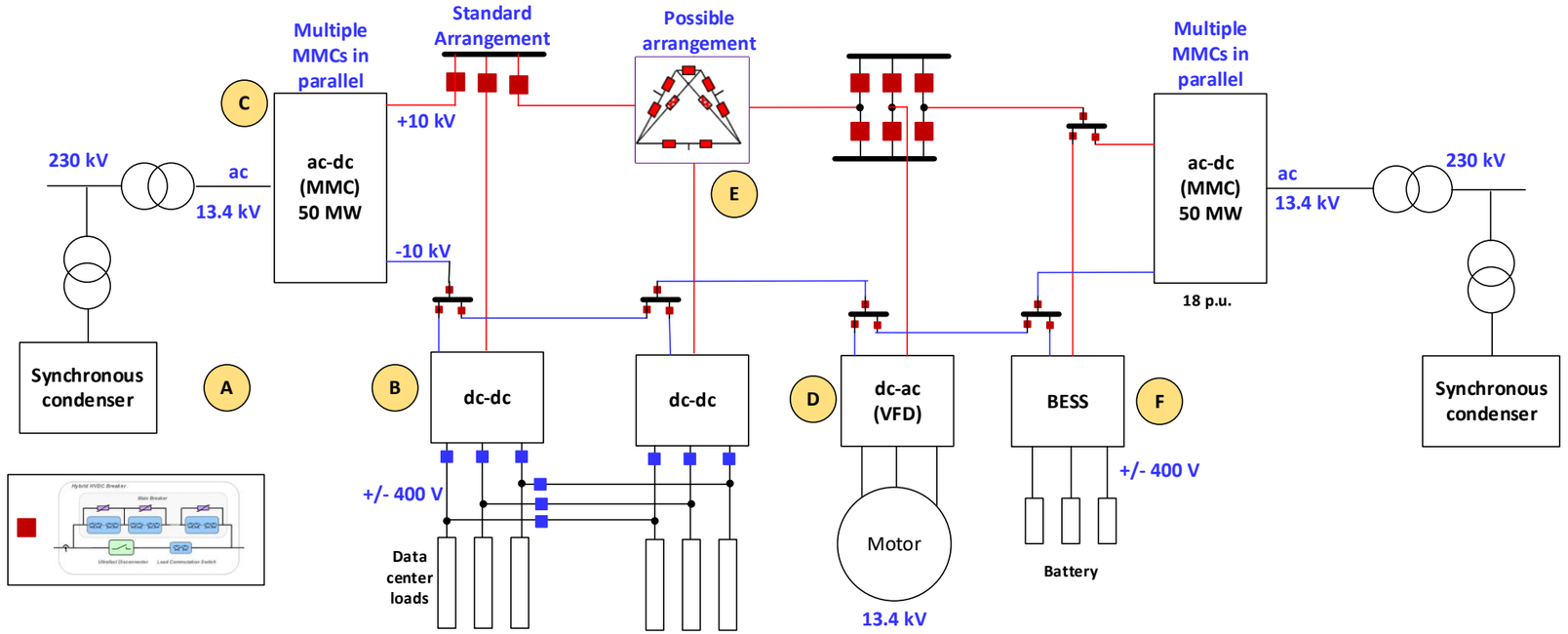
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The MMC is a Clear Choice to Enable this MVDC Grid

- MMC is a well matured and proven technology in applications – it represents a **scalable, matured, well-understood architecture for establishing high power dc voltages**

- Modular in nature and can operate seamlessly even under submodule failure

- Deployment of the MMC to establish the dc grid permits additional controllability in establishing the dc system, similar to the benefits offered by the proposed in the 800V data center concept



A Architecture with Reliable design

B dc-dc converters with multiple low voltage loads

C MMC control under parallel connection, weak ac network GFM features

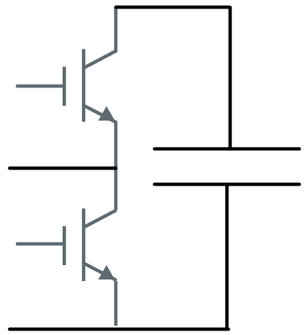
D MMC control for VFD

E Protection of multi-terminal dc system [5]

F BESS: Jitter control

- Extreme power density requirements of data centers motivate MMC miniaturization – this is the goal of our project.

Miniaturization of the MMC Submodule



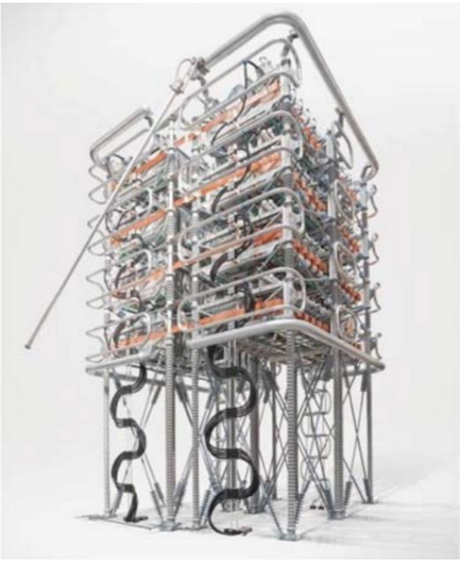


SM without capacitor

SM w/ capacitor



Converter tower



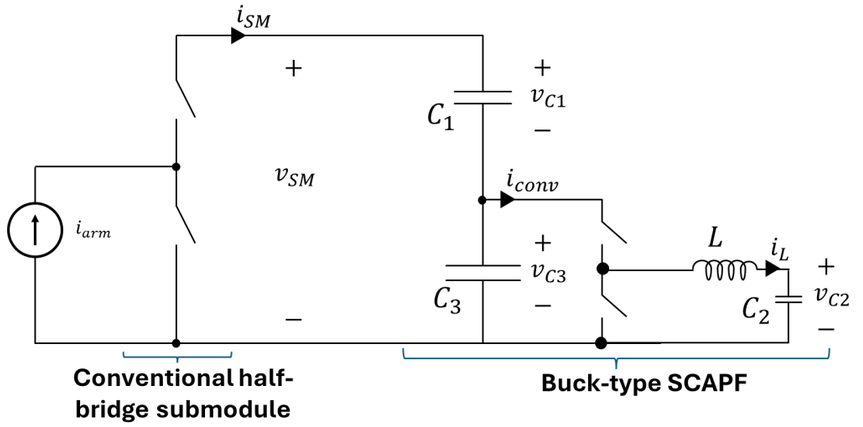
- **Benefits of miniaturization are immense**: higher power density, reduced footprint (paramount for offshore substations), simplification of deployment and installation
- **Challenge:** the MMC's volume is dominated by the submodule capacitor
  - ~60% of the volume, dictates submodule geometry and tower layout [6]
  - Capacitor provides line-frequency harmonic power buffering and system energy storage
- **Opportunity:** Advance new, practically achievable, low-cost wide band gap (WBG)-enabled active power filter (APF) circuit architectures that can mitigate this bottleneck
- **Project Summary:** Reduction of foot-print, weight, volume and cost of Modular Multilevel Converter for Data Center Applications through design of Active Power Filter based Submodules, employing SiC Devices
- **DOE Alignment:** Aids to the sustainable growth of upcoming Data Center Loads

SM Miniaturization

a) **Employ active power filters (APFs):** within every submodule, most common implementation in the literature being a buck converter – this increases the hardware complexity but can achieve maximum miniaturization of the MMC submodules

b) **Employ a centralized APF:** suppress circulating currents without burdening the conventional control of the MMC.
Achieving lower capacitance reduction than if these APFs are deployed in every submodule.

Focusing on ‘a’



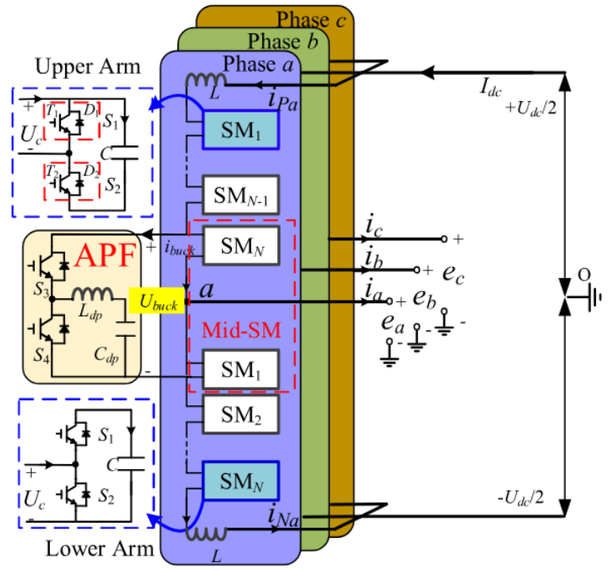


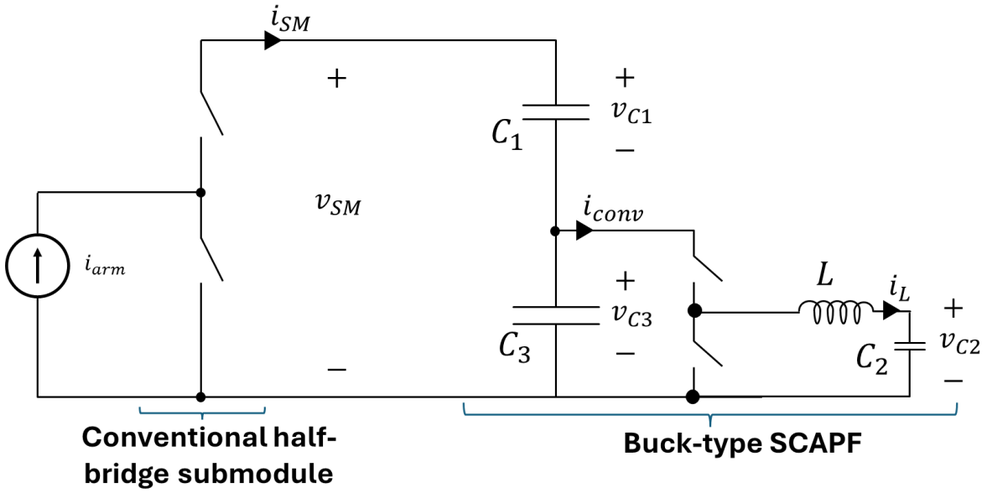
Fig. 1. Configuration of the modified APF-MMC topology.

[7]

Series Capacitor APF (SCAPF) Design Framework

- This project investigates the use of the Series Capacitor APF (SCAPF), which is based on a class of series-stacked capacitor buffer active power filters which have been previously investigated for low-power single-phase ac/dc conversion applications, but have not been considered for the MMC.

- **Key advantages**:
  1. Permits usage of lower voltage APF switches, which have higher figures-of-merit and permit faster switching to miniaturize overall APF
     - Key disadvantage of traditional Buck-APFs
  2. Decouples V_{SM} from voltage ripple on any one capacitor, permitting larger voltage swings and thus lower energy storage (lower volume)



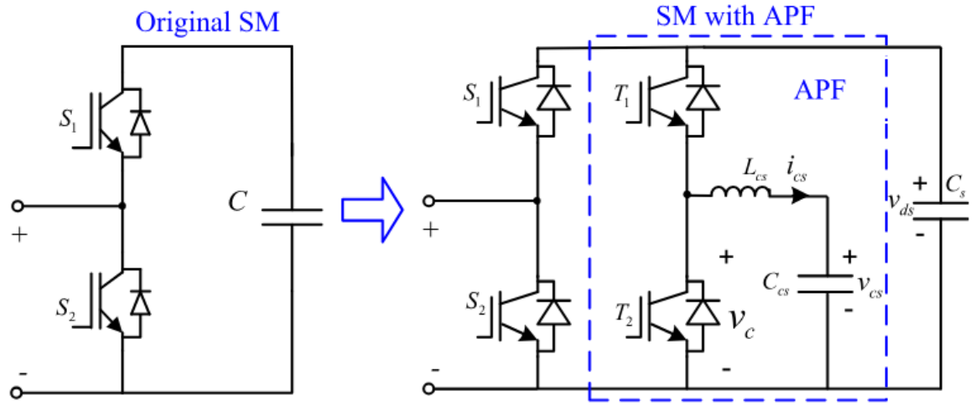


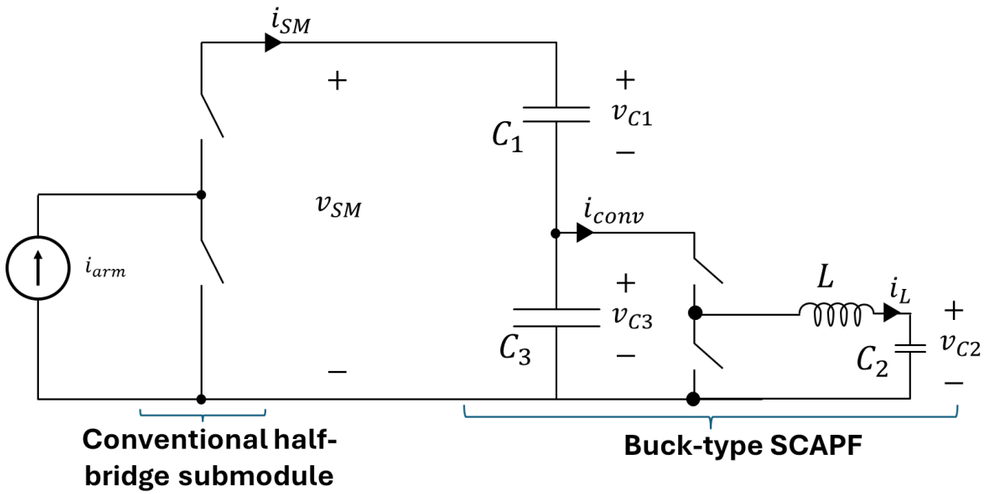
Fig. 3. Proposed MMC SM with active power decoupling.

[8]

APF Design methodology

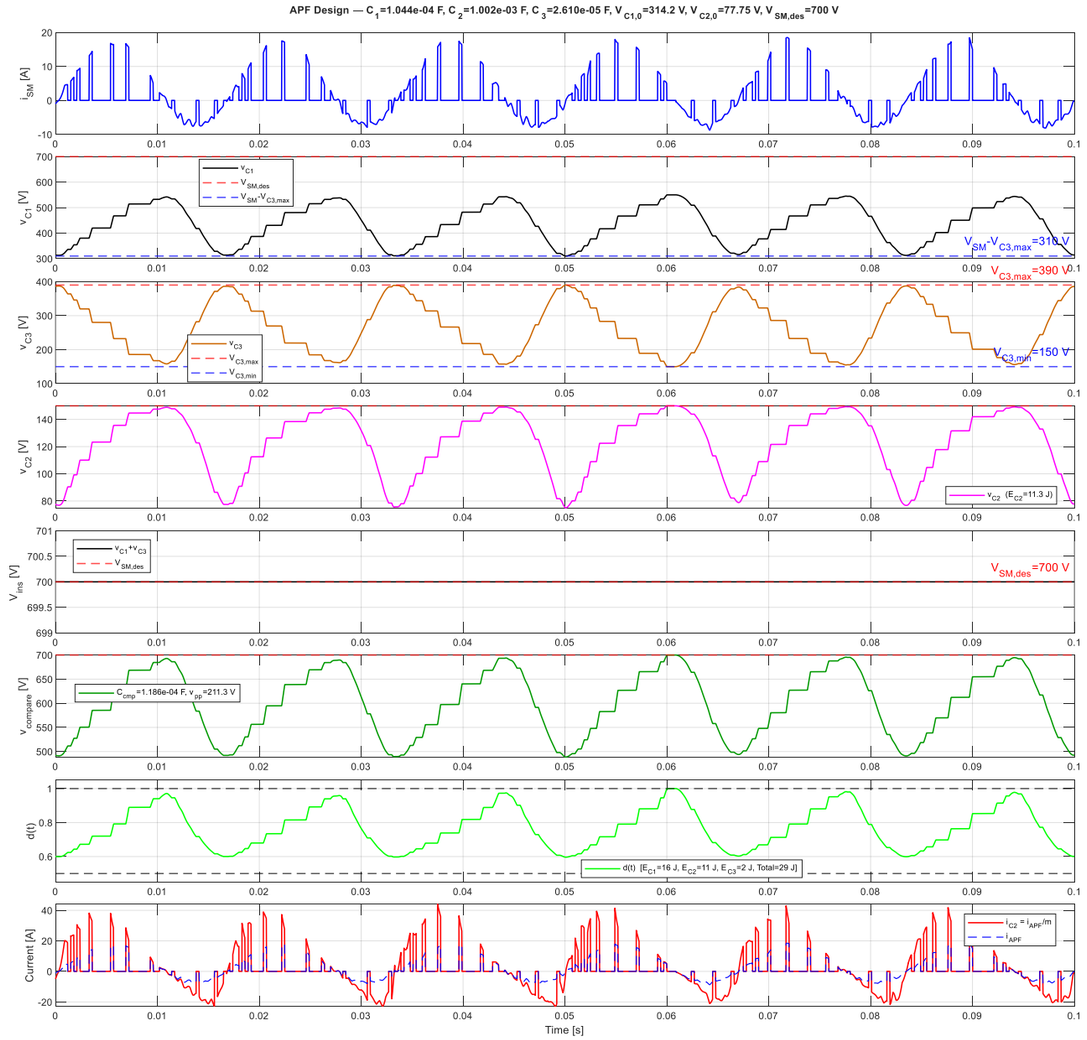
Inputs:
- SM current
- Desired max/min capacitor voltages

Outputs:
- Capacitance values for minimum energy storage (max. miniaturization)
- Operating voltage and currents
- Nominal converter duty cycle command



APF for hardware prototype: Simulation Results

Parameter	Value	Comment
SM Voltage, v_{SM}	700V	Representative blocking voltage for a 1.2kV IGBT at 60% derating.
RMS submodule current	5A	200x derating over nominal system rms current.
SM Switch Voltage Rating	1.2kV	IGBT, standard voltage blocking
SM Switching Frequency	500Hz	Matching nominal SM operation in ORNL MMC simulation.
SCAPF Switch Voltage Rating	650V	SiC, targeting $v_{C3,max} = 390V$. Lower voltage blocking compared to SM IGBTs permits demonstration of higher figure-of merit switches
SCAPF Switching Frequency	2kHz	Higher than SM switching frequency to demonstrate benefit of fast-switching SiC. To be refined with switching simulations.
RMS SCAPF current	12A	Extracted from APF design tool.
C1	$104.4\mu F$, 550Vmax	Output from APF design tool. Net stored energy of 30.4 J. An equivalent traditional submodule has 2.8x higher energy storage – this demonstrates the substantial miniaturization potential.
C2	$1mF$, 150Vmax	
C3	$26.1\mu F$, 390Vmax	
L	$100\mu H$	Target to be refined with switching simulations.



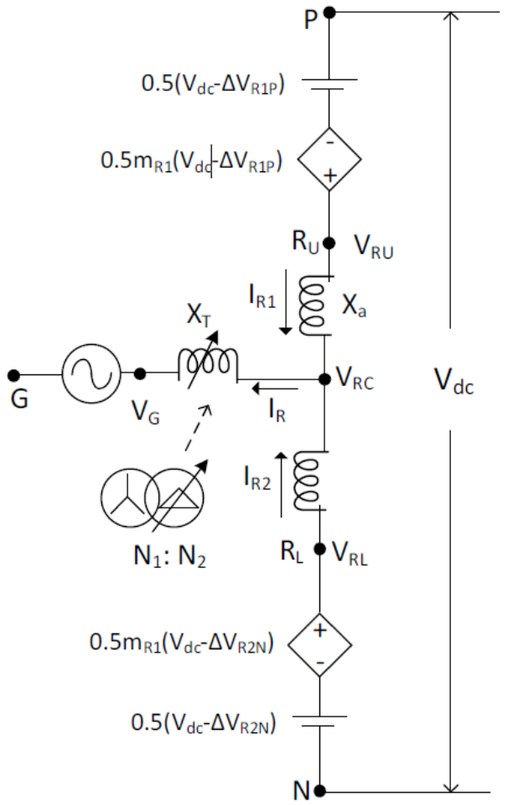
APF design tool outputs for selected operating configuration.

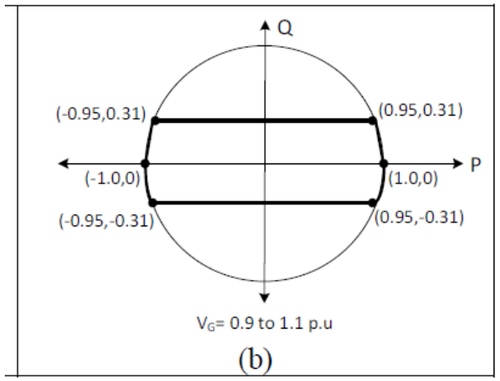
MMC Design Criteria for Data-Center Applications

- MMCs are widely deployed in High-voltage DC (HVDC) applications
- Supposed to comply with grid codes
- P-Q capability under varying grid voltage (0.9 to 1.1 p.u)
- The operating point does not vary quickly in HVDC systems
- Tap changing transformer is used to adjust the ac voltage seen by MMC

- In Data Centers, the load fluctuates very quickly
- Tap-changer operates very slow
- Hence, not feasible for Data-Center Applications

- Approach:
  - Fix the DC voltage
  - Reduce the nominal secondary voltage of the transformer to meet the P-Q capability
  - Results in higher MMC arm currents, higher loss





[9]

Design Verification through Simulation Study

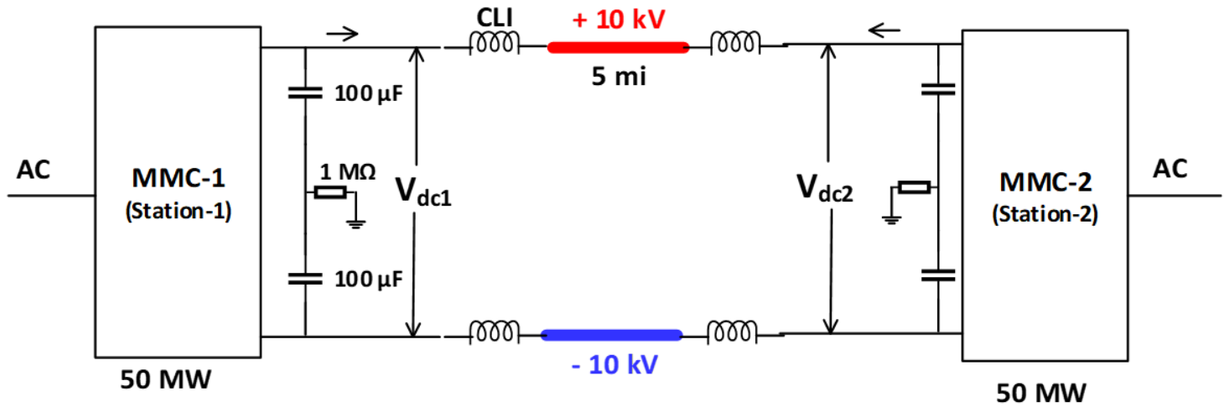


Fig. 2. Point-to-point MMC system.

AC voltage	13.8 kV line-line rms
Transformer Secondary voltage	10.63 kV
DC voltage	±10 kV
Number of submodules per arm	20
Voltage of each sub module	1000V
Sub module capacitance	27.8 mF (33 kJ/MVA)
Average switching frequency of each submodule	12*60 = 720 Hz
Converter rating	50 MW
Reactive power	16.5 MVar
Transformer	52.5 MVA, 15% inductance
Arm inductance	12% of transformer base

Staion-1: DC voltage control mode
Station-2: AC power control mode
Power flow from Station-1 to Station-2

Traditional Half-Bridge SM

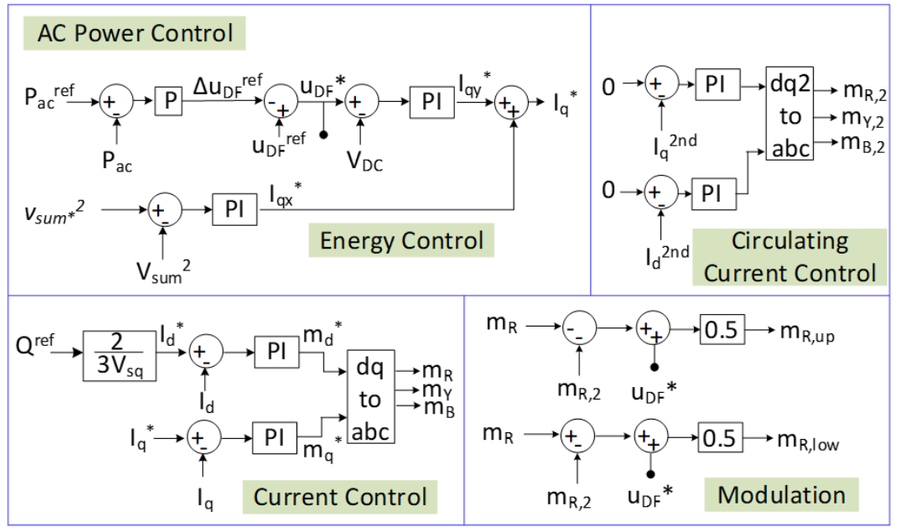
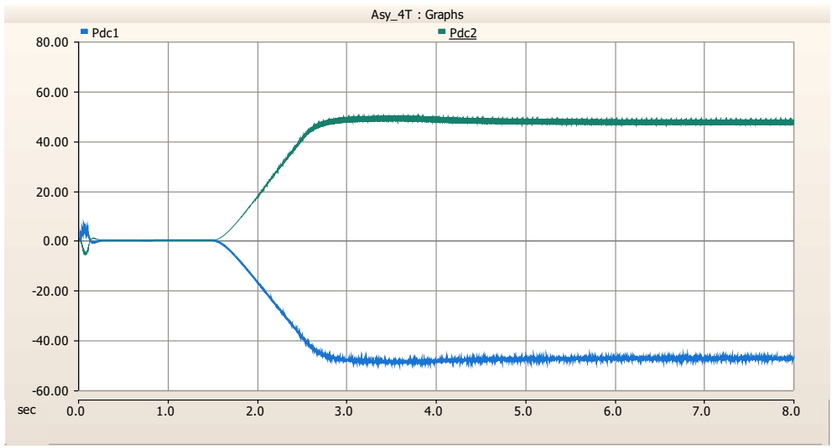
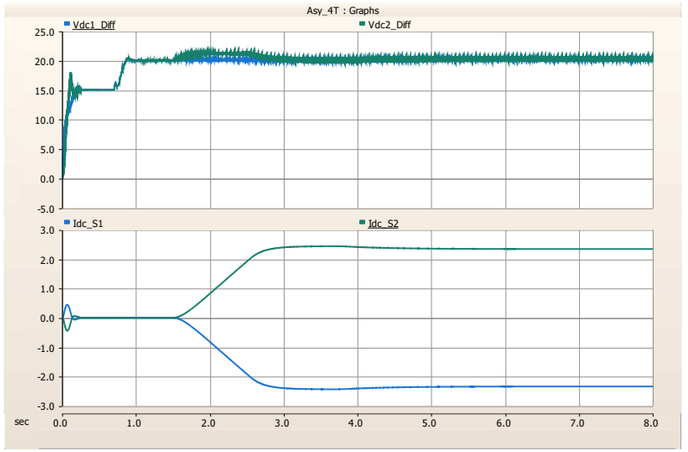


Fig. 3. Control block diagram of MMC.

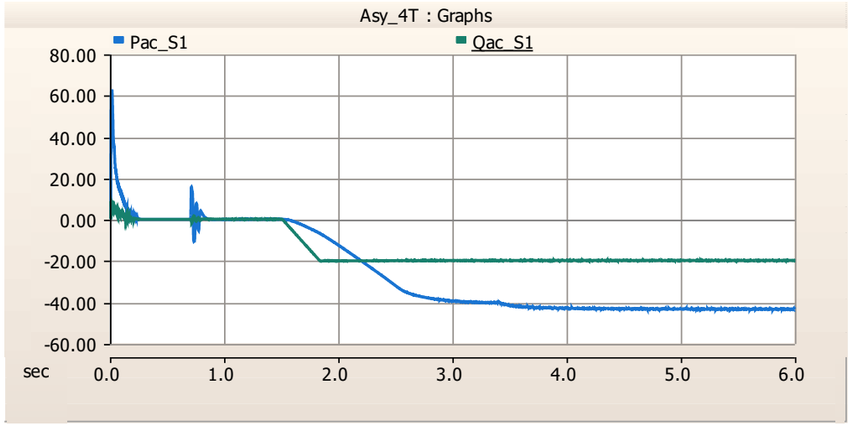
Simulation Results



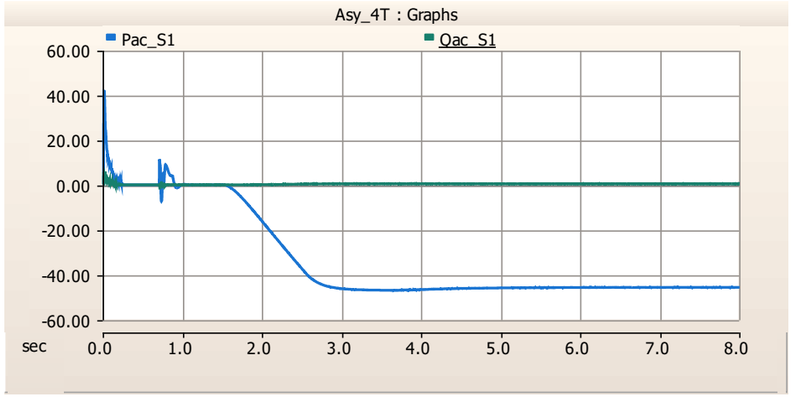
DC power



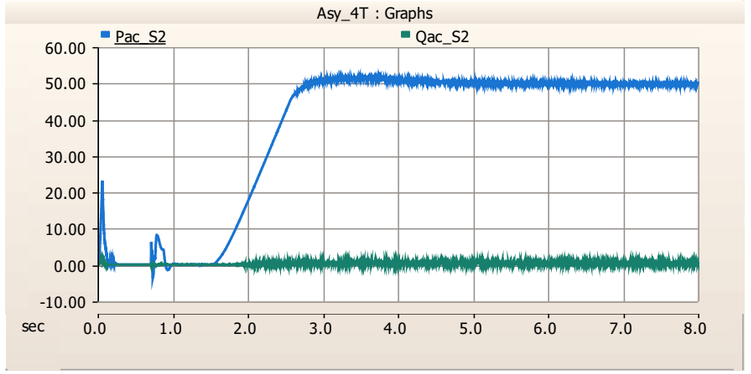
DC voltage and current



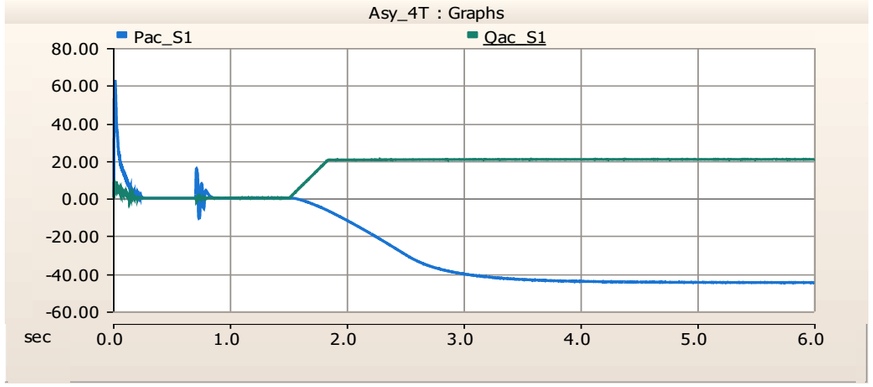
Station-1 (-0.95, -0.33)



AC power: Station-1 (-1.0, 0)



AC power: Station-2 (-1.0, 0)



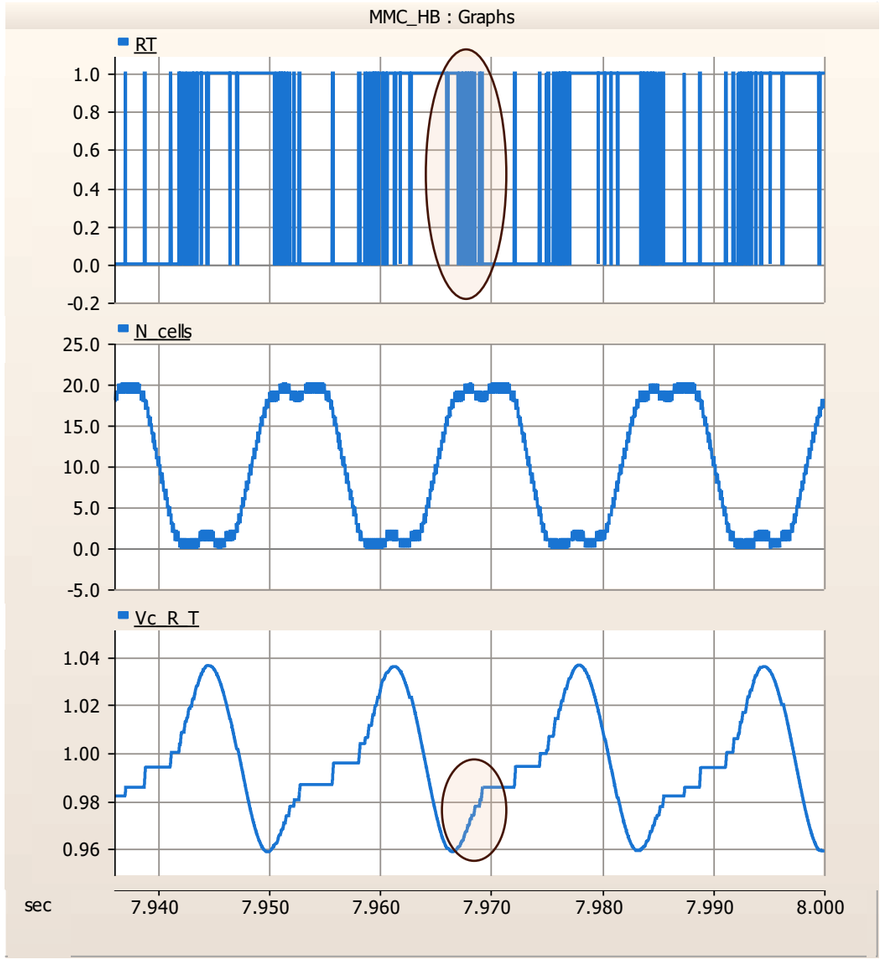
Station-1 (-0.95, 0.33)

Switching Logic[1]

- In HVDC systems each MMC arm contains hundreds of Submodules (SM)
- Each SM operates at very low switching frequency (around 1-2 times fundamental frequency)

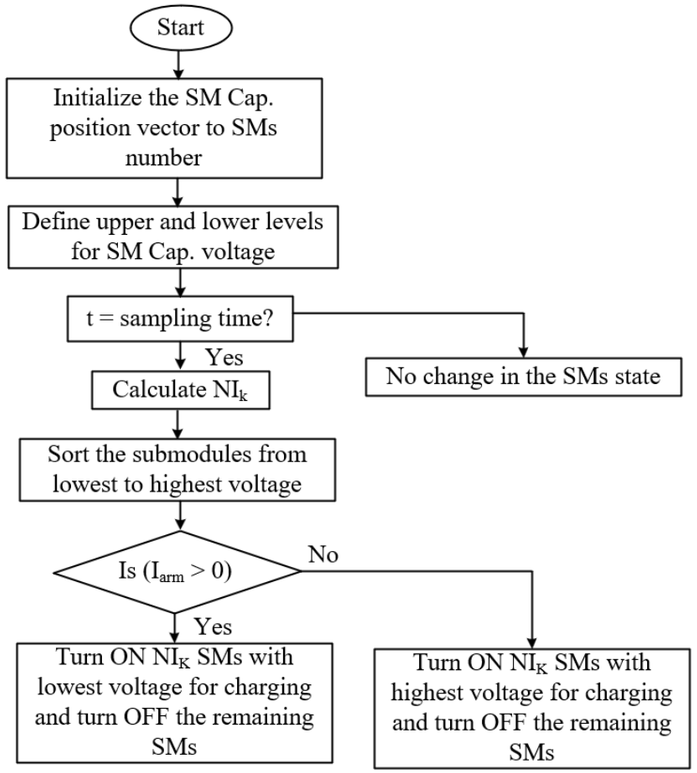
- In Data-Center MMC, lower number of SMs per arm (N=20 here)
- Manage SM voltage balance and reduce switching frequency

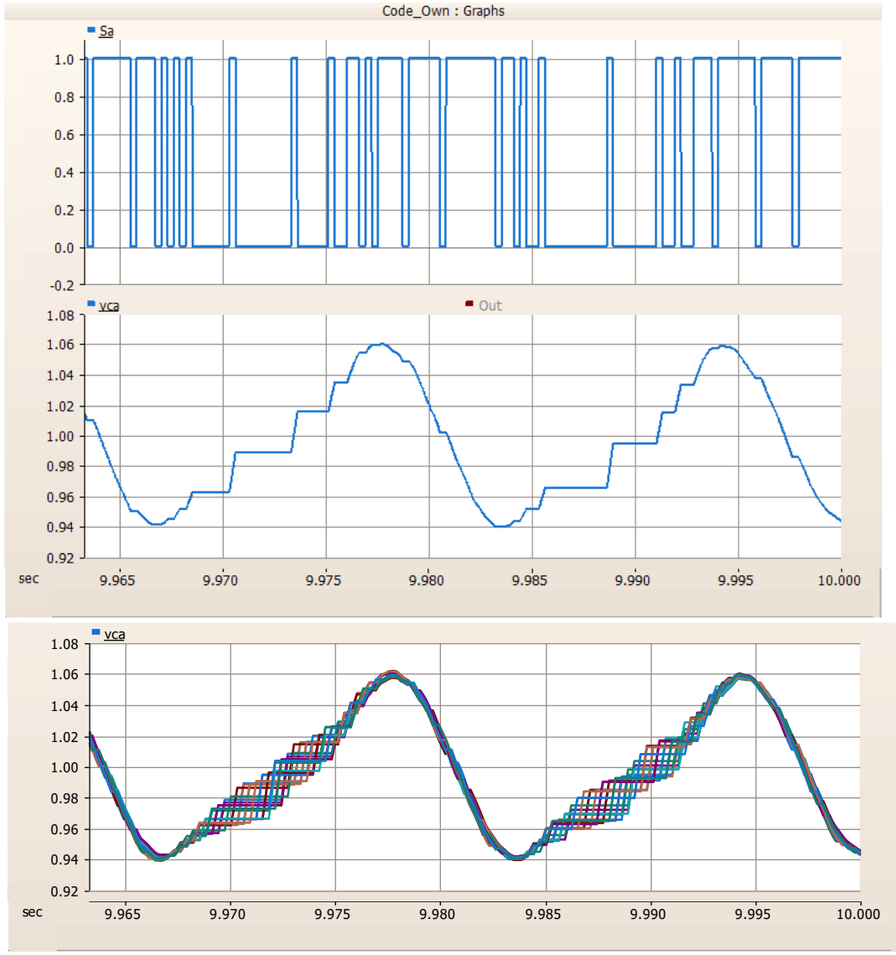
- Default sorting and cell balancing algorithms from PSCAD is implemented
- Resulting in undesirable submodule switching



Switching Logic[2]

- The switching logic shown is implemented
- Average switching frequency is 720 Hz





I_{arm}: MMC arm current

Nest steps:

Offline simulations
- Design APF for 50 MW MMC
- Incorporate APF based SM in the simulation model
- Verify the performance under steady-state, dynamics and fault conditions

Hardware prototype
- Selection and procurement of hardware components
- Prototype Development and Testing

HIL Simulations
- Development of 50 MW MMC real-time model with standard HB SMs
- Development of 50 MW MMC real-time model with APF SMs
- Integration of hardware prototype with the ARISE platform and testing

References

1. J. E. Ontiveros, xAI's Colossus 2 - First Gigawatt Datacenter In The World, Unique RL Methodology, Capital Raise, en, Sep. 2025. Accessed: Oct. 29, 2025. [Online]. Available: https : / / newsletter.semianalysis.com/p/xais-colossus-2-first-gigawatt-datacenter.
2. J. E. Ontiveros, AWS Trainium3 Deep Dive — A Potential Challenger Approaching, en. Accessed: Jan. 26, 2026. https://newsletter.semianalysis.com/p/awstrainium3- deep-dive-a-potential.
3. D. Patel, Multi-Datacenter Training: OpenAI's Ambitious Plan To Beat Google's Infrastructure, en. Accessed: Jan. 26, 2026. https://newsletter.semianalysis.com/p/ multi-datacenter-training-openais
4. NVIDIA 800 VDC Architecture for AI Data Centers, en-us. Accessed: Mar. 27, 2026. https://www.nvidia.com/en-us/data-center/technologies/800-vdcarchitecture/.
5. Vishal Vekhande, J. Sivaprasad, Vinothkumar K, Sridhar Alapati, Jwala Rao, Saikat Karmakar, "A Generalized Procedure to Develop DC Switchyard for MTDC Grids", Electric Power and Energy Conference (EPEC), Edmonton, Canada, Nov. 2020. https://ieeexplore.ieee.org/document/9320124
6. K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for Transmission Systems*. John Wiley & Sons, 2016.
7. *Jia, Guanlong, Min Chen, Song Tang, Chenghao Zhang, and Bin Zhao. "A Modular Multilevel Converter With Active Power Filter for Submodule Capacitor Voltage Ripples and Power Losses Reduction." IEEE Transactions on Power Electronics 35, no. 11 (2020): 11401–17. https://doi.org/10.1109/TPEL.2020.2982440.*
8. *Kong, Zenghui, Xin Huang, Ze Wang, Jian Xiong, and Kai Zhang. "Active Power Decoupling for Submodules of a Modular Multilevel Converter." IEEE Transactions on Power Electronics 33, no. 1 (2018): 125–36. https://doi.org/10.1109/TPEL.2017.2661539.*
9. Sreenivasa S Jaldanki, Y. Agalgaonkar, M. Ranjram, "Design of Medium-Voltage Modular Multilevel Converter (MMC) for Data Center Loads without Tap-changing Transformer", Letters, IEEE Transactions on Power Electronics", under review

Thank You

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