Presentation Submission Information

- **Presentation ID#:** 4.1
- **Presentation Title:** 3-D Double-Sided Isolated 10 kV/300 A Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Power Module with Embedded Active Gate Driver and Jet Impingement Cooling
- **Author(s):** Faisal Khan, Gilbert Moreno, and Shuofeng Zhao
- **Organization(s):** National Laboratory of the Rockies (NLR), North Carolina State University (NCSU), University of Texas at Austin (UT), University of Wisconsin at Milwaukee (UWM).



National Laboratory of the Rockies

U.S. DEPARTMENT of ENERGY

3-D Double-Sided Isolated 10 kV/300 A SiC MOSFET Power Module with Embedded Active Gate Driver and Jet Impingement Cooling

Faisal Khan

National Laboratory of the Rockies (NLR)

September 22, 2026

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Project at a Glance

Project Description: This project develops a power dense 10 kV and 300 A half bridge power module for solid-state transformer (SST) applications.

Period of Performance: 9/1/2025 to 9/30/2028

Award Amount: $1,200,000 (DOE)

Prime Awardee: National Laboratory of the Rockies

Partners: North Carolina State University (NCSU), University of Texas at Austin (UT), University of Wisconsin at Milwaukee (UWM).

Technology Areas:

- Advanced Transformers
- DC Circuit Breakers
- Advanced Power Electronics

Alignment/Supports strategic pathway:

- Our 10kV SiC module implemented in future SST designs can bring the following improvements:
- Stabilize: Provide real time insights and coordinated response support, while the high-performance 10 kV SiC power module enables faster, more resilient SST operation during reliability events.
- Optimize: Enhance grid performance and security through analytics and monitoring, with the SiC module improving efficiency, power density, and overall SST capability.
- Grow: Support innovation and future ready grid development by simplifying SST implementation and enabling integration of advanced technologies through the SiC module’s high-voltage, high-performance design.

Problem Statement: Motivations

- Solid-State Transformers (SSTs) are essential for modernizing the U.S. grid so it can support bidirectional power flow, integrate rapidly growing renewable energy, and meet the intense localized demands of AI data centers and EV fast-charging infrastructure.
- The proposed power **300A** SiC half bridge power module provides true **10 kV** blocking in a single module, while SOTA IGBTs top out at **6.5 kV** and cannot reach 10 kV without series stacking.
- Its fast switching allows SSTs to operate in the medium-frequency range of approximately 5–20 kHz, compared to high-voltage IGBTs that are typically limited to about 1–3 kHz, enabling significantly smaller and lighter medium-frequency transformers.
- It delivers lower conduction and switching losses than silicon or SiC IGBTs, even compared to the highest-current IGBT modules (up to **1800–3600 A** but only at **≤6.5 kV**).
- It simplifies SST design by eliminating voltage-balancing networks required for series-stacked IGBTs in medium-voltage stages.
- It creates a compact, high-power building block ideal for MVDC grids, renewables, and next-generation SSTs where single-device 10 kV capability is critical.
- **Commercial IGBT technology cannot match the 10 kV voltage, switching speed, or efficiency of a SiC MOSFET**, making this module fundamentally superior for modern SST architectures.

Key Innovations

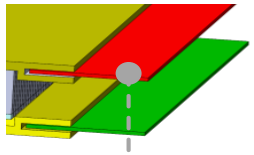
A 10 kV / 300 A SiC MOSFET Power Module with Integrated Jet Impingement Cooling

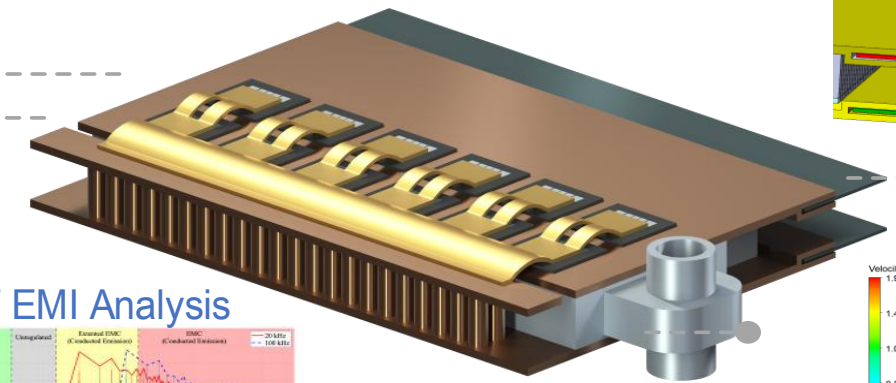
Program Objectives: Develop a 10 kV/ 300 A SiC MOSFET power module with embedded jet-impingement cooling and active gate driver

Embedded Active Gate Driver



Pocket busbar

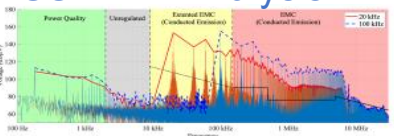




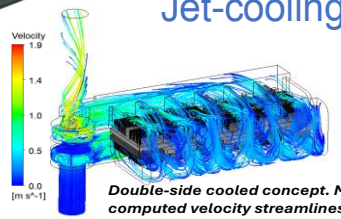
SST Verification



SST EMI Analysis



Embedded Jet-cooling



Double-side cooled concept. Model computed velocity streamlines

Technical Approach

- Embedded jet-impingement cooling
- Active gate drivers for current sharing
- Pocket-type terminal-busbar interface

Technical Challenges

- High thermal resistance due to insulation
- Current imbalance between chips in parallel
- Partial discharge and reliability

Features

- State-of-the-art highest current rating 10 kV/300 A SiC power module
- Embedded thermal management
- Balanced current sharing

Deliverables

- Plug-and-play MV SiC solution
- 10 kV power module modeling, fabrication, insulation verification
- SST level EMI modeling and mitigation

Impacts

- Enhanced SST power capability
- Innovative MV power module layout
- Multiple-level connection for beyond 20 kV applications
- Paving the way for MVDC power grids

EMI= Electromagnetic interference

Project Schedule and Milestones



Power module design, fabrication, and testing (NLR, NCSU)

Active gate driver design, fabrication, and testing (UT Austin)

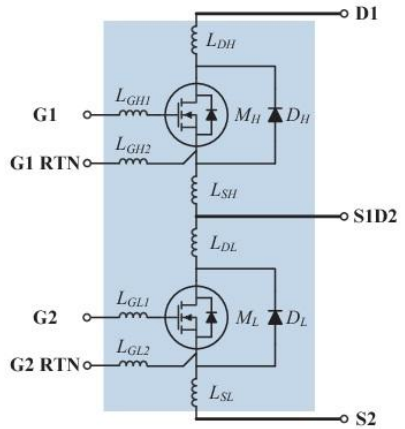
Electro magnetic interference analysis (UW Milwaukee)

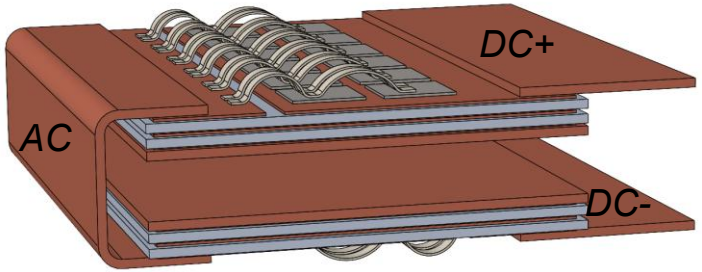
Module loss calculation (NCSU)

SST implementation (NCSU)

Module Packaging Strategies

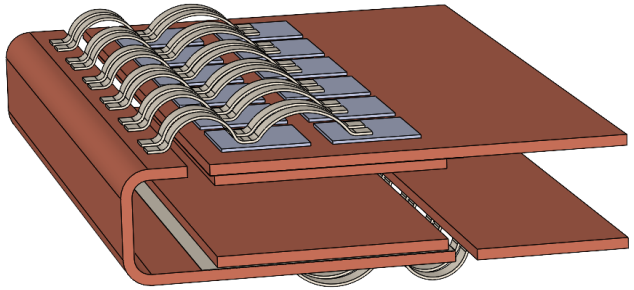
Evaluated various implementations of the half bridge power module

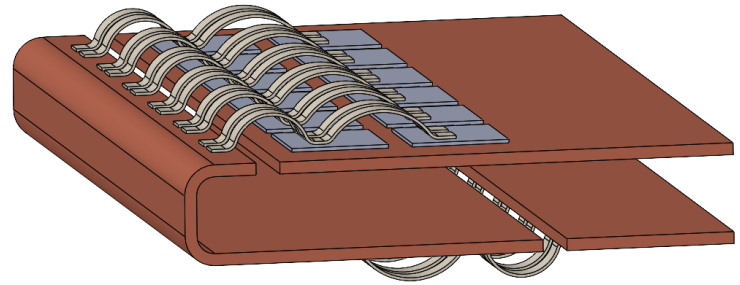




Metallized ceramic substrates and water-based coolant (e.g., water-propylene glycol mixtures)

- Baseline design





Thin dielectric coating and water-based coolant

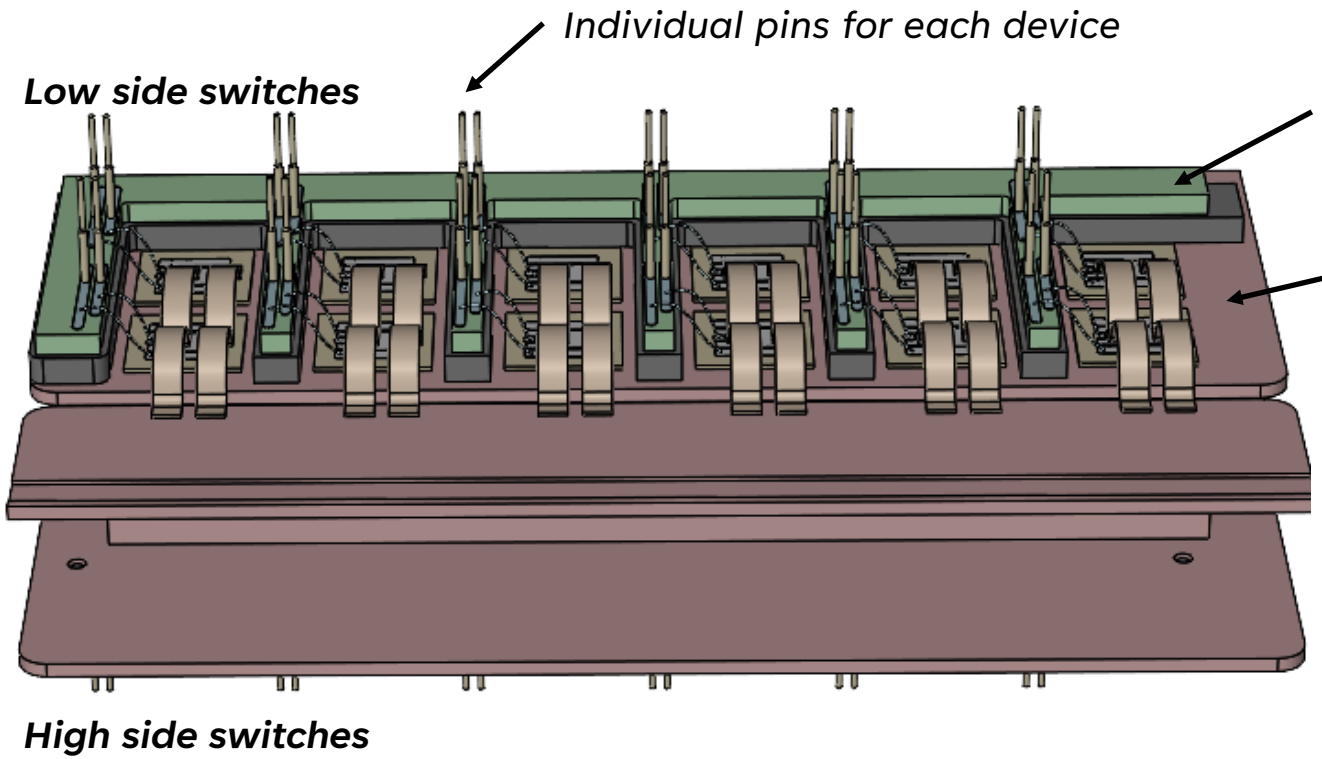
Considered Temprion and aluminum oxynitride (AlON) dielectric coatings

Dielectric fluid coolant

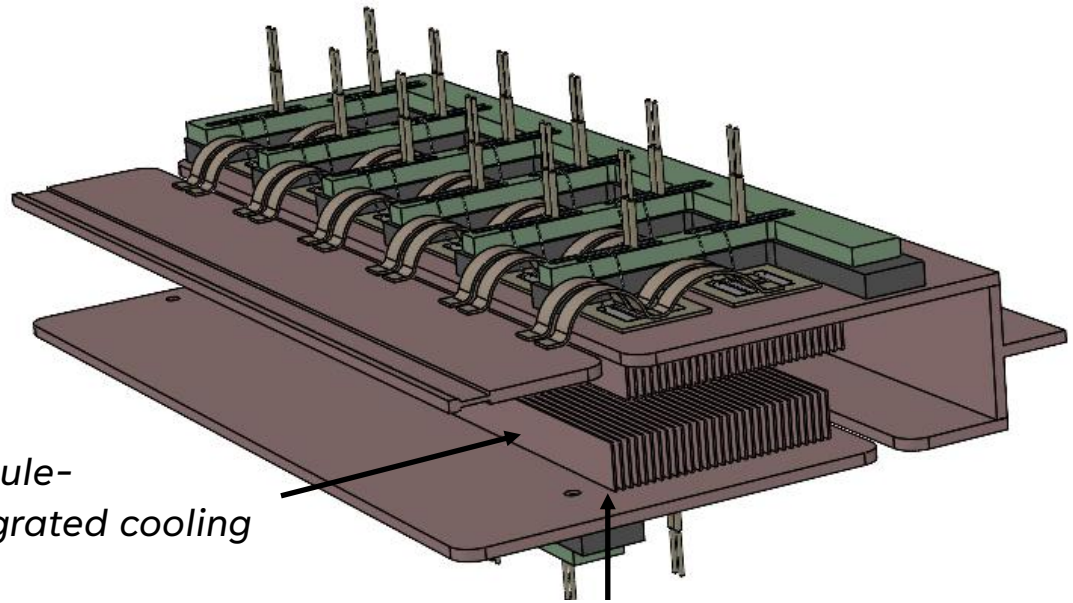
- **Eliminates the need for dielectric materials such as ceramics resulting**
- **Simplifies packaging**

Both concepts have been evaluated. Pursued the dielectric fluid cooled module architecture due to its simplified packaging, lower cost, and improved thermal performance

Finalized Module Structure

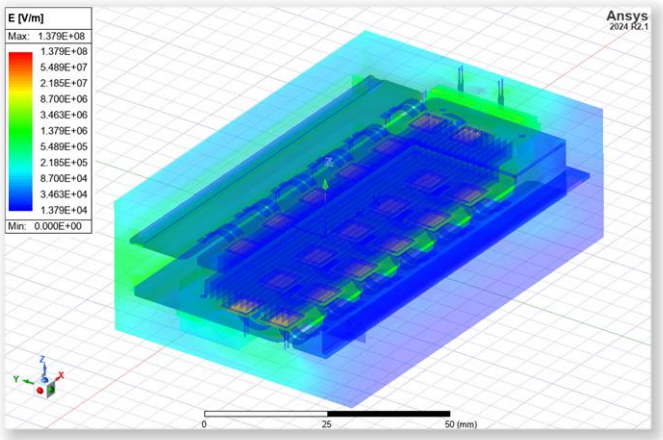


- Module design is compatible with both dielectric fluid and water-based coolant
- Will pursue the dielectric fluid module for this project

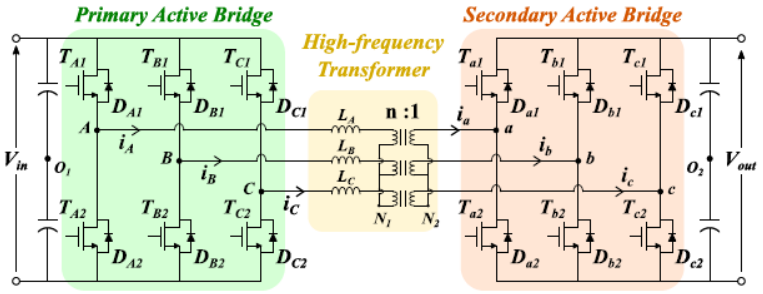


Power Module Electrical Design Approach

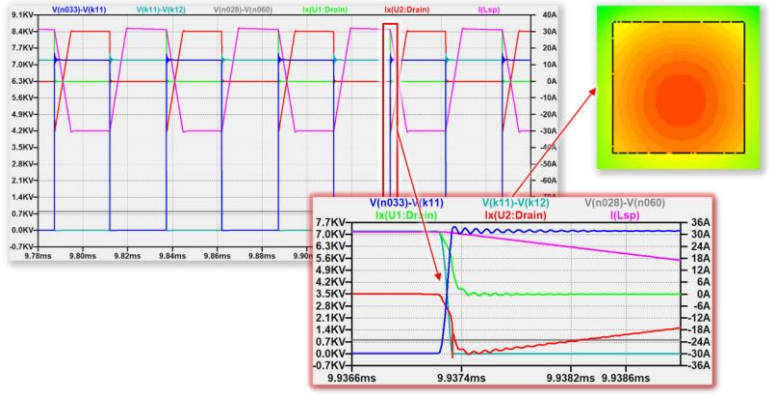
Design the package layout and compute electrical parasitic values and electric field potential (**NLR**)



Provides SST operating conditions for the 10 kV power module (**NCSU**)

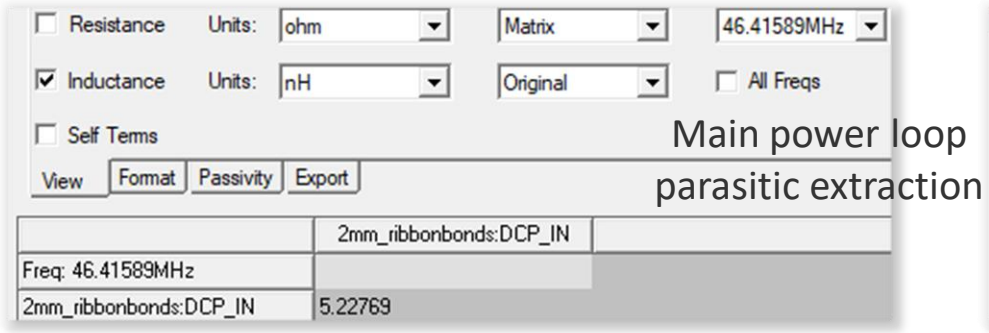


Assesses the heat loss of the power module when operating in an SST environment (**NLR**)



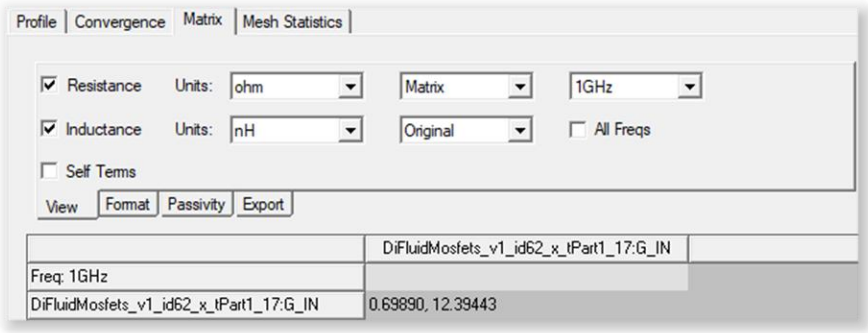
Simulation Results: Power Module's Parasitic Extraction

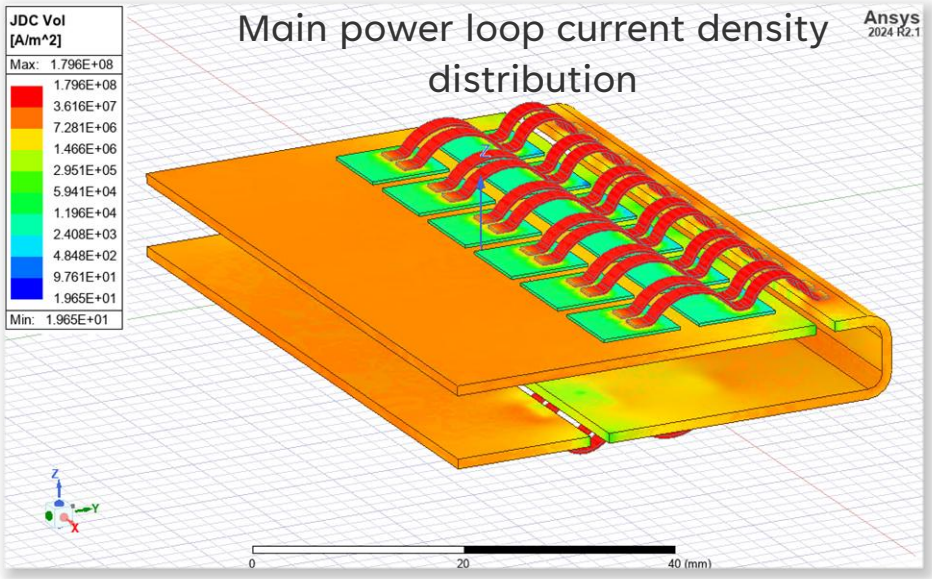
Dielectric fluid cooled module

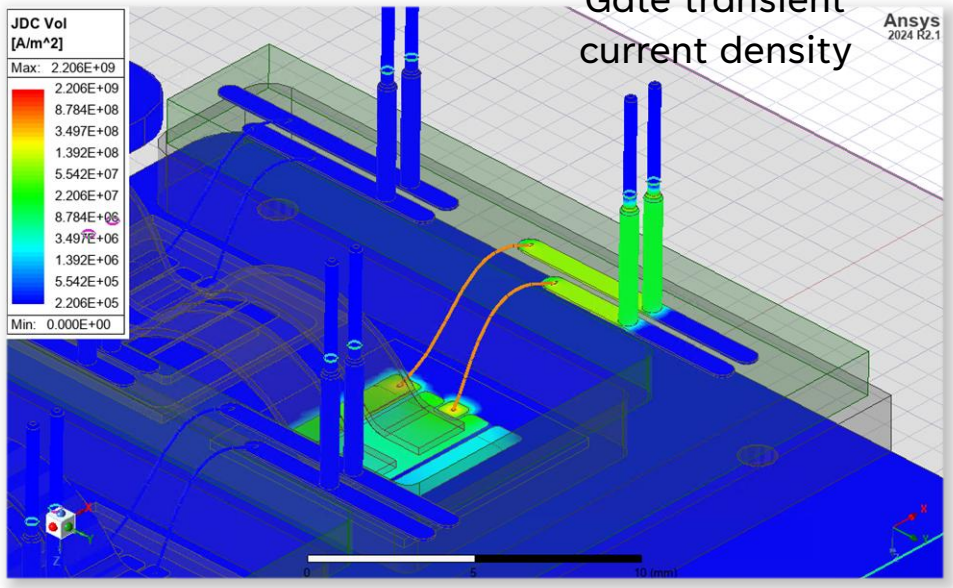


Main power loop parasitic extraction

Gate loop parasitic extraction



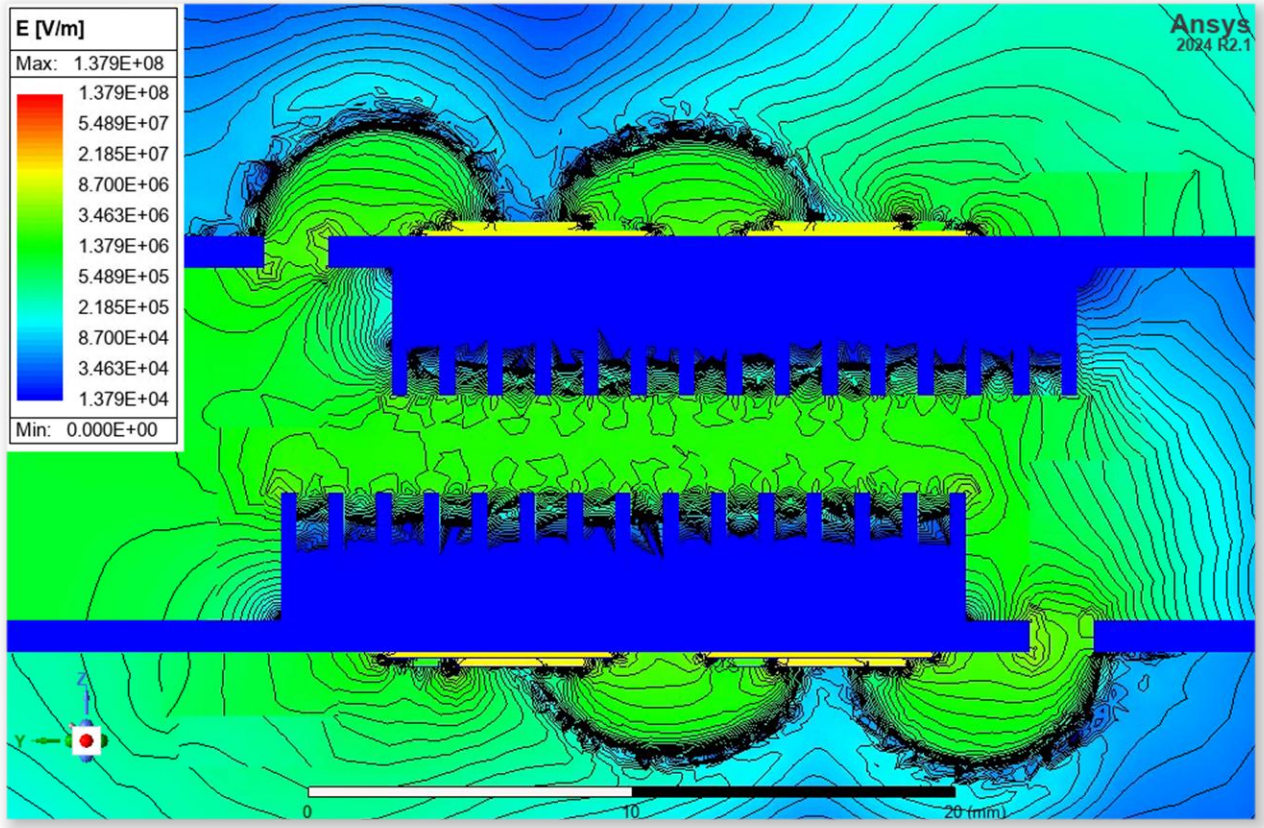


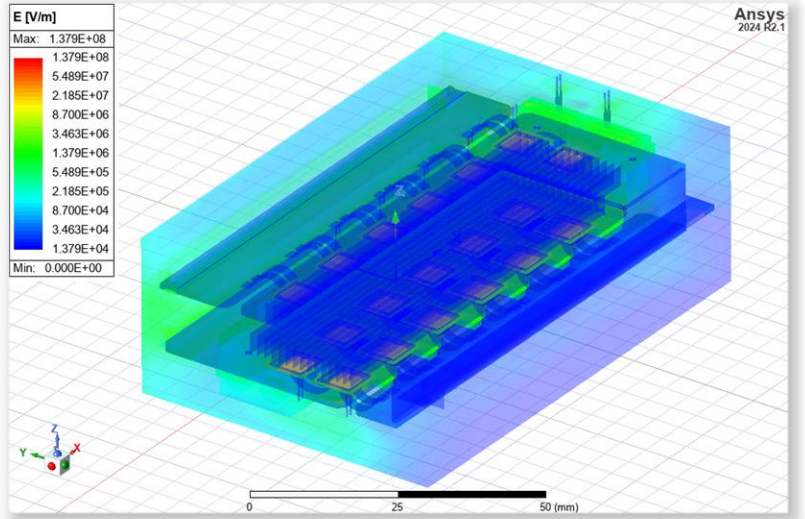


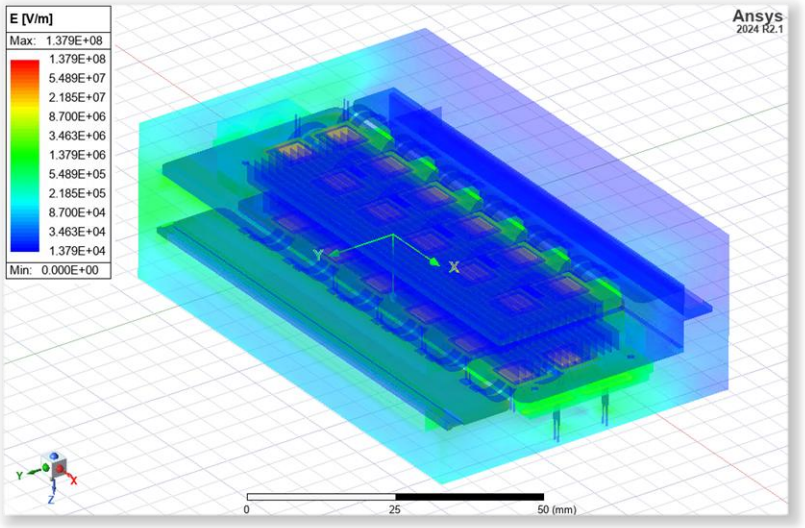
Computed module parameters for future system-level simulations

- Main power loop inductance: **5.2 nH** (total)
- Gate loop inductance: **12.4 nH** (per die)

Simulation Results: Electric Field Potential







Upper and lower positions OFF

- **Simulated E-filed distributions**
- **E-field strength are well under 30kV/mm, the reliable operating number for state-of-the-art encapsulants**

Simulation Results: Power Module Loss Estimates

```
%% Post Processing 001 -- Truncate 002 -- 20kHz
oe_trac_results_tiv_lite_01 = readtable('OE_TRAC_DAB_Circuit_v001.txt');

% oecif_results_tiv_index_011_lite_01 = 1;
% oecif_results_tiv_index_012_lite_01 = 1000001;

% oecif_results_tiv_index_021_lite_01 = find(oecif_results_tiv_lite_01.time == 0, 1, "first");
%oecif_results_tiv_index_021_lite_01 = find(oecif_results_tiv_lite_01.time >= 0.000176908, 1, "first");

oe_trac_results_tiv_index_021_lite_01 = find(oe_trac_results_tiv_lite_01.time >= 0.009, 1, "first");
oe_trac_results_tiv_index_022_lite_01 = find(oe_trac_results_tiv_lite_01.time == 0.01, 1, "last");

%% Power Switches Losses -- Truncate 002 -- 20kHz
%%%%%%%%%% Switch UU %%%%%%%%%%
oe_trac_results_tloss_uu_lite_01 = sum(abs((oe_trac_results_tiv_lite_01.V_n033__V_k1
                                            oe_trac_results_tiv_lite_01.Ix_U1_Drai
                                        )) / (oe_trac_results_tiv_index_022_lite_01

%%%%%%%%%% Switch UL %%%%%%%%%%
oe_trac_results_tloss_ul_lite_01 = sum(abs((oe_trac_results_tiv_lite_01.V_k11__V_k12_
                                            oe_trac_results_tiv_lite_01.Ix_U2_Drai
                                        )) / (oe_trac_results_tiv_index_022_lite_01

oe_trac_results_tloss_uu_lite_01
oe_trac_results_tloss_ul_lite_01

(oe_trac_results_tloss_uu_lite_01 + oe_trac_results_tloss_ul_lite_01)/2.0
```

- **Power module operating at 7.2 kV, 300 A**
- **17.4 kW module heat dissipation**

Entry	Value
Power loop inductance (nH)	5.6
Gate loop inductance (nH)	14.0
Decoupling capacitance (nF)	5.0
External gate resistance (forward/reverse) (Ω)	5.0/2.5
1-device-per-position loss (W)	1451
Power module loss (W)	17413

Thermal Design

- Selected dielectric fluid cooling for the power module. This configuration:
  - Eliminates the need for electrically insulating layer/material → **improved thermal performance**
  - Simplifies fabrication → **lower cost**

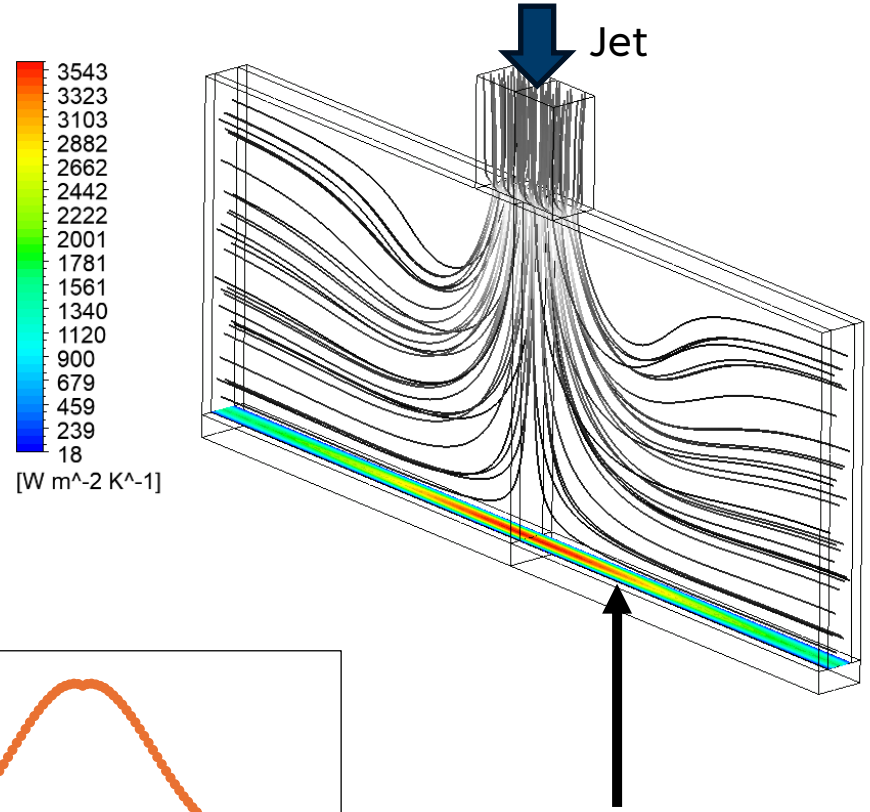
- Use jet impingement to increase the heat transfer coefficients and offset the poor properties of the dielectric fluids.

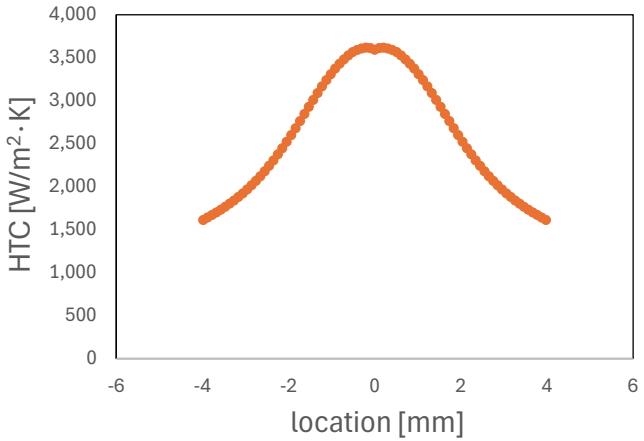
Fluid *(properties at 40°C)*	Thermal conductivity [W/m-K]	Specific heat [J/kg-K]	Density [kg/m^3]	Viscosity [Pa-s]	Flash point [°C]	Pour point [°C]	Dielectric Strength [kV]	Dielectric constant (ASTM D924)
EC-110 * (dielectric fluid)	0.137	2,212	820	0.00595	203	-60	>60	2.1
PGW (30% vol.)	*0.43*	*3,860*	*1,023*	*0.0025*	*> 104*	*-13 (freeze point)*	-	*~50*

* https://www.engineeredfluids.com/products/electrocool

PGW: propylene glycol -water

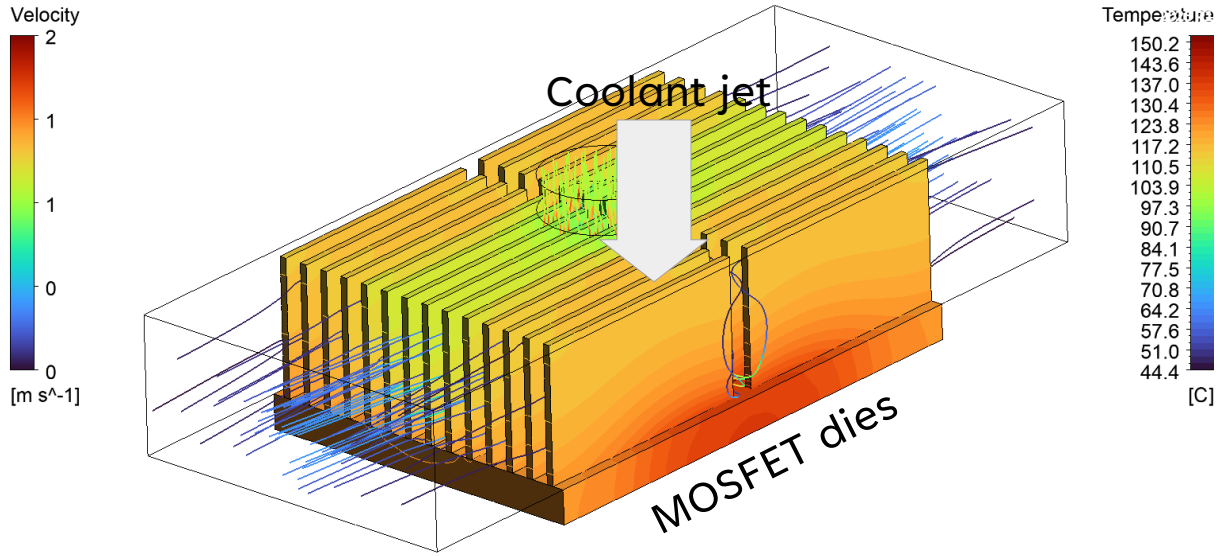
Simulation Results: Coolant Flow





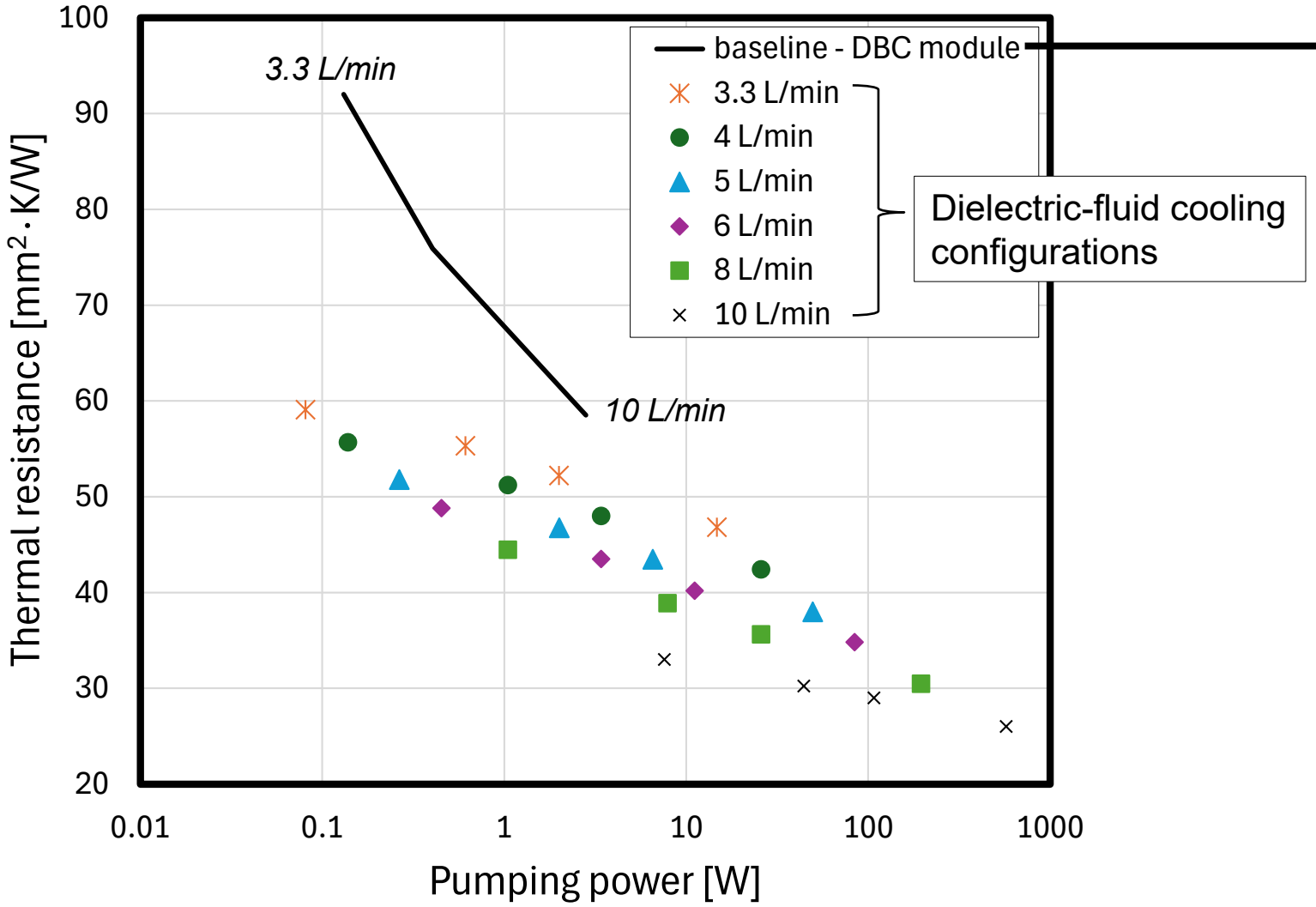
Highest heat transfer coefficients at the impingement zone

Use jets to increase heat transfer coefficients [2]

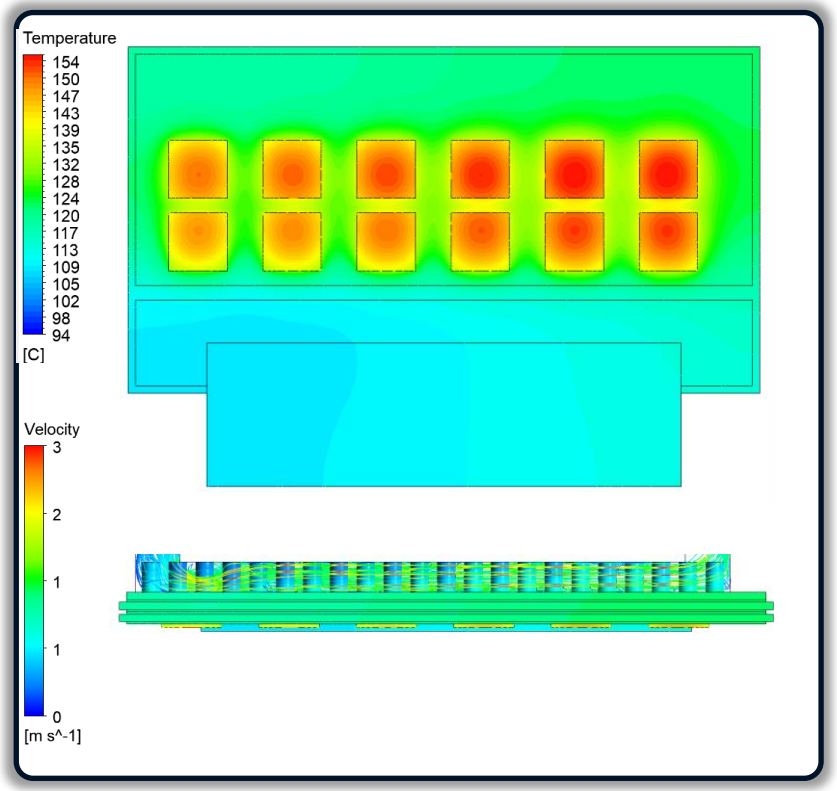


Impinge dielectric fluid jets directly behind each device → high heat transfer coefficient directed at the heat source

Simulation Results: Impact of Pumping Power



Predict improved thermal performance and lower pumping power using the dielectric fluid concept



Baseline module: Direct bonded copper (DBC) substrate using water-based coolant and pin-fin cold plate

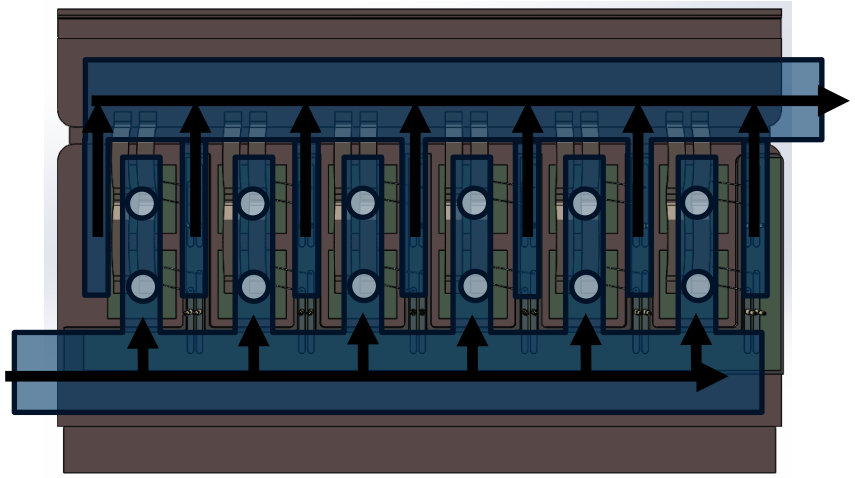
Conclusions & Key Findings

- Completed the electrical design of a 10 kV, 300 A power module. The module offers the highest in-class current rating, uses an active gate driver technology to ensure even current sharing among devices, and has integrated cooling.
- Modeled the performance and heat loss of the 10 kV module under SST operation. Calculated heat dissipation per half-bridge module is ~**17kW**.
- Developed a dielectric fluid cooling concept that uses jet impingement to augment thermal performance. The dielectric cooling design is predicted to provide both a lower thermal resistance and pumping power compared with a metallized ceramic base module.
- **Verdict 1: Dielectric-coolant-based thermal management delivers superior thermal performance compared to DBC structures using water-based coolants.**
- **Verdict 2: Initial simulation results confirm a safe breakdown field below 30 kV/mm across the power module.**

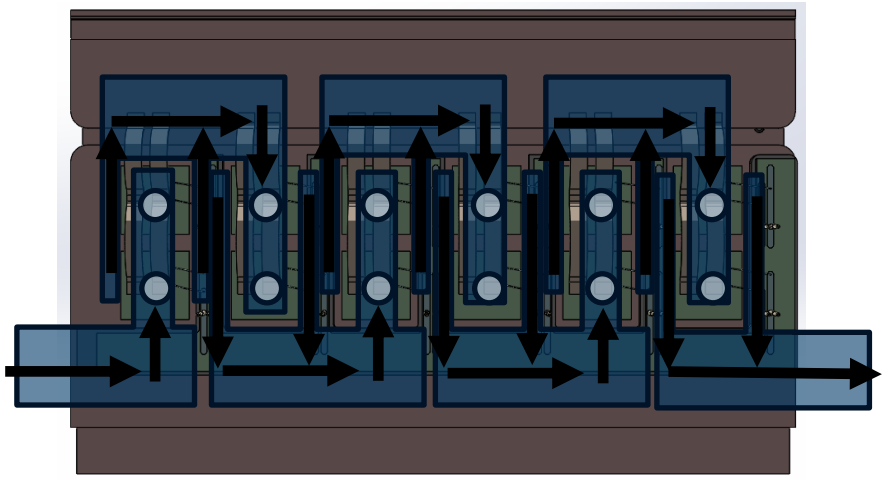
Future Steps

- Complete the design for the dielectric fluid cooling system.
- Complete the active gate driver design fabrication [3].
- Fabricate a power module prototype using 10kV bare dies from wolfspeed.
- Develop the electromagnetic interference (EMI) model [4].

Parallel flow configuration



Series flow configuration

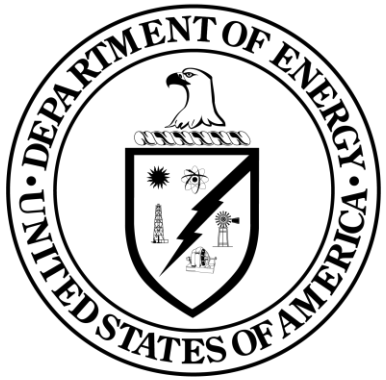


References

- [1] X. Li, Y. Chen, H. Chen, R. Paul, X. Song and H. A. Mantooth, "A 10 kV SiC MOSFET Power Module with Optimized System Interface and Electric Field Distribution," in IEEE Transactions on Power Electronics, vol. 39, no. 8, pp. 9540-9553, Aug. 2024.
- [2] G. Moreno, S. V. J. Narumanchi, K. S. Bennion, R. M. Kotecha, P. P. Paret, and F. Xuhui, “Jet impingement manifolds for cooling power electronics modules,” Issued Patent U.S. 11,751,365 B2, Sep. 05, 2023.
- [3] X. Zhou, Z. Liang and A. Huang, "A High-Dynamic Range Current Source Gate Driver for Switching-Loss Reduction of High-Side Switch in Buck Converter," in IEEE Transactions on Power Electronics, vol. 25, no. 6, pp. 1439-1443, June 2010.
- [4] T. Li, R. Olson, H. Abdallah, N. Sivadanam and R. M. Cuzner, "Modeling and Validation of Common-mode Emissions of Silicon Carbide Enabled Motor Drive in Extended EMC Frequency Range Between 2 kHz and 30 MHz," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 2904-2911.
- [5] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya and K. Hatua. "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," in IEEE Transactions on Industry Applications, vol. 51, no. 4, pp. 3343-3360, July-Aug. 2015.

Acknowledgements

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