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Office Of Nuclear Energy
Sensors and Instrumentation
Annual Review Meeting

Radiation Hardened Circuitry Using Mask-Programmable Analog Arrays

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ORNL

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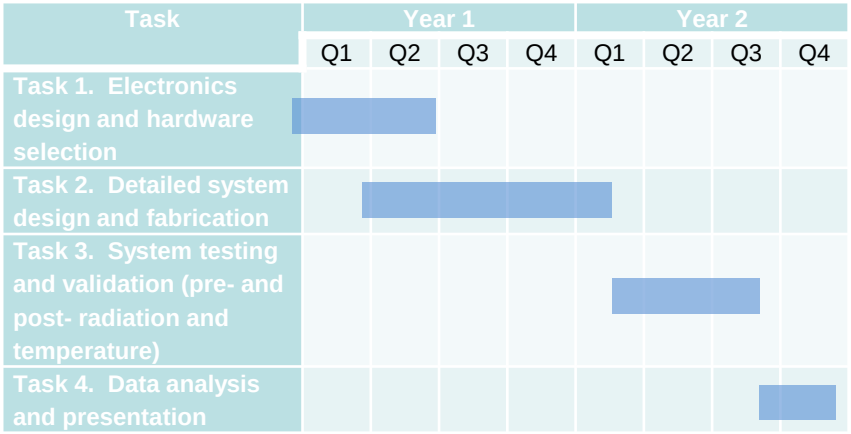
Project Overview

- **Goal, and Objectives**
  - This project will develop and demonstrate a general-purpose data acquisition system built from commercial or near-commercial radiation-hard analog arrays and digital arrays that will be the building blocks of a family of future fieldable radiation-hard systems.
- **This project is complementary with the ASU project**
- **Participants**
  - Jacob Shelton (UT student), Nance Ericson, Miljko Bobrek – ORNL
  - Benjamin Blalock – The University of Tennessee
- **Schedule**



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Accomplishments – FY14 Tasks

Task 1. Electronics design and hardware selection (year 1, month 5) – This design task will result in a report containing diagrams and functional descriptions of all system components, to be delivered to the sponsor.

Task 2. Detailed system design and fabrication (year 2, month 2) - This design task will produce all completed circuit schematics of the system including the necessary files for printed circuit board fabrication and system fabrication. The system will be fabricated and tested for functionality. Any design revisions will be made at this time. At the completion of this task a report will be delivered to the sponsor detailing the system design and results of the preliminary testing.

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Accomplishments – FY15 Tasks

- Task 3. System testing and validation (pre- and post- irradiation and temperature) - Evaluation of the performance of the system for both pre- and post-irradiation as well as operation at elevated temperature will be performed. Detailed performance of the system will be documented to ensure the design meets requirements prior to any extended evaluation.

- Task 4. Data analysis and presentation - Data taken from the pre- and post-radiation/temperature evaluation will be analyzed to quantify variations. Measured performance changes will be identified and the root cause at the circuit level will be determined. This will give us a good measure of the overall performance of the system that can be clearly communicated to potential users of this technology.

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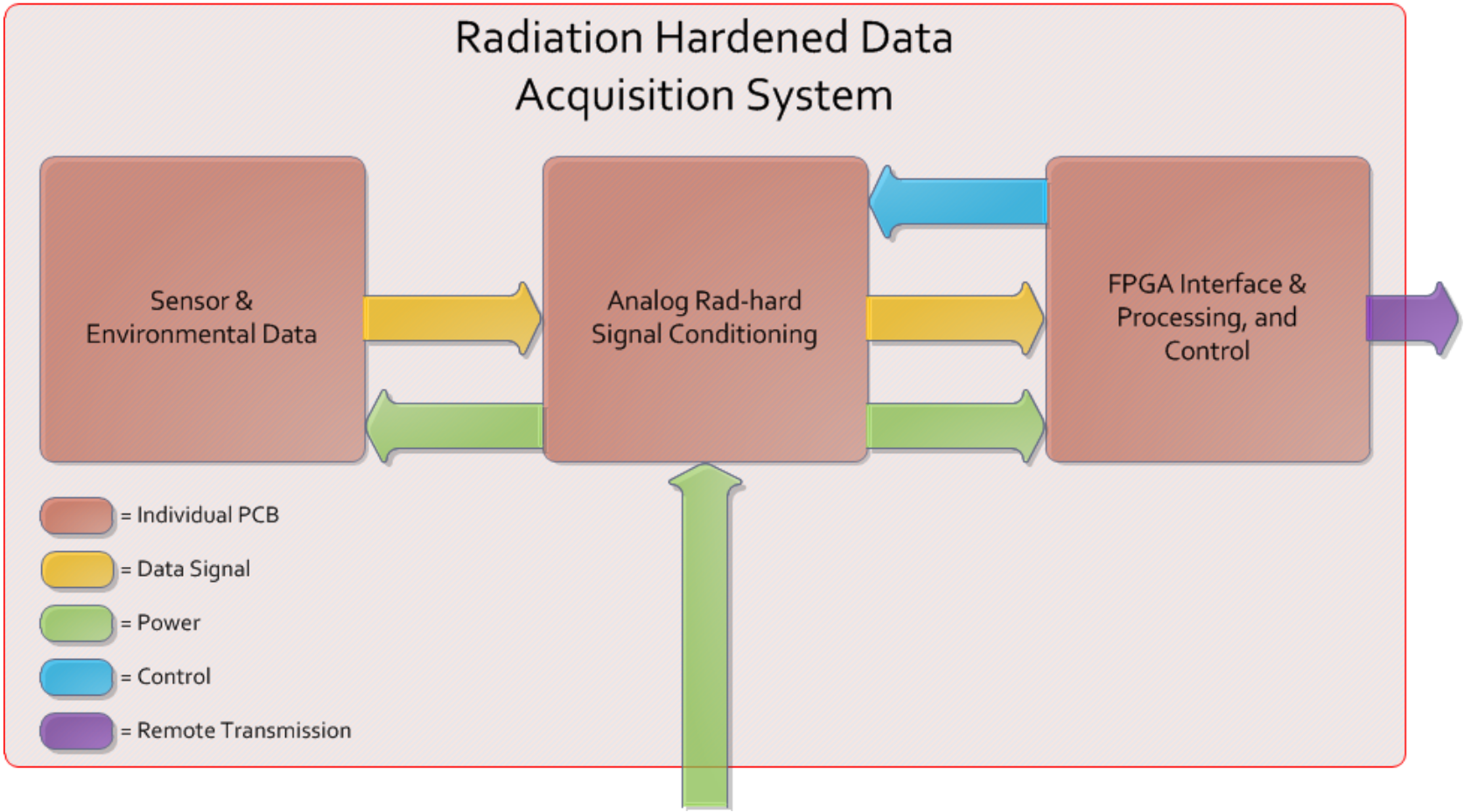
Accomplishments – Hardware System Overview



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Accomplishments – Hardware System Details

Sensor Board

Power to Sensor Board

Data from Sensor Board

Rad-Hard Board

Power Supply/ Battery

Data to/from Rad-Hard Board

Interface Board

USB Data Cable

Nexys 3 Board

110V-5V converter

The system is currently operational from end-end.

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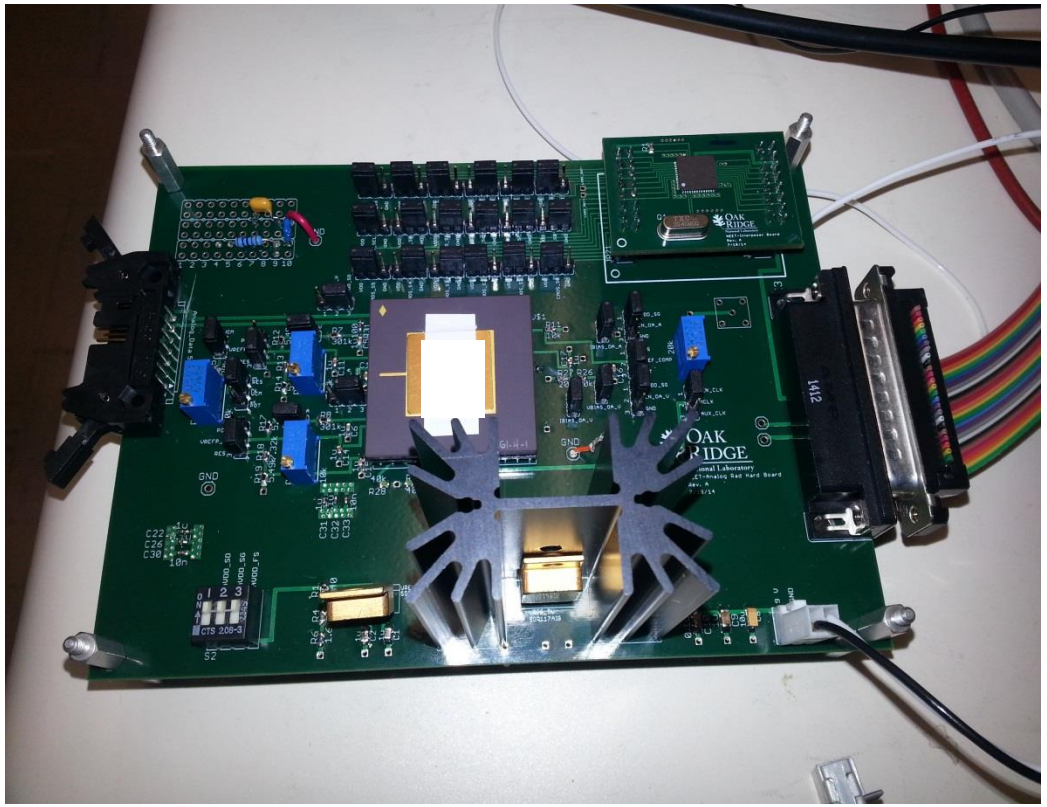
Accomplishments – Rad Hard Board

- **The Rad-Hard Analog Board is the heart of the system.**
- **It contains:**
  - Triad Semi rad-hard Via-Configured Analog Array (VCA)
  - Frequency Management International (FMI) Synthesizer
  - MicroSemi Voltage regulators
- **Triad VCA implements:**
  - Two 2nd-order sigma-delta (SD) analog-digital converters (ADC)
  - Comparator
- **FMI Synthesizer is the ADC clock generator**



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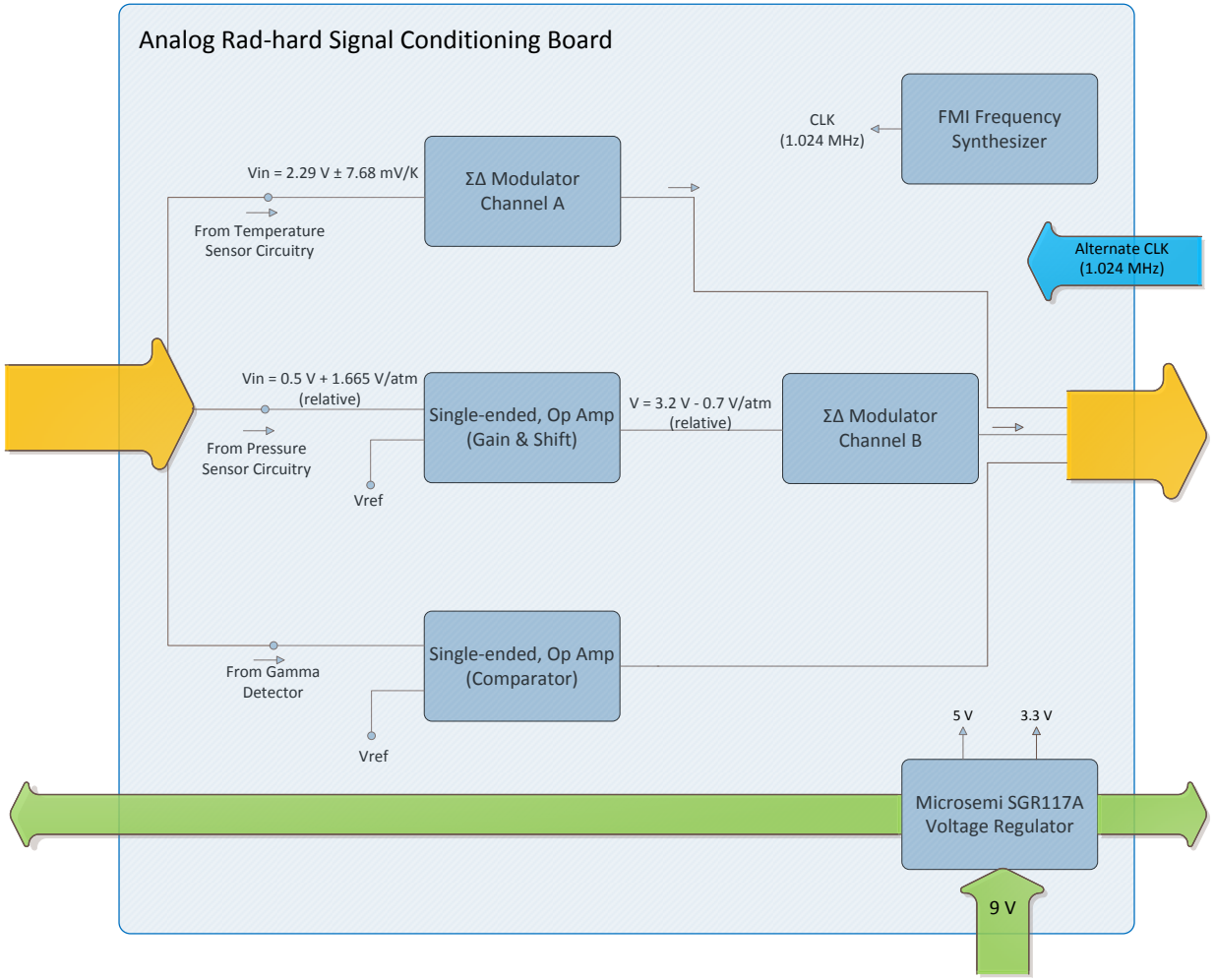
Accomplishments – Rad Hard Board

- The VCA ASIC has a great deal of functionality we did not use.
- The two SD modulators take the analog data and generate a bitstream.
- The comparator takes the pulse from the Geiger tube and generates a logic-level pulse for the FPGA.
- The frequency synthesizer generates the 1 MHz sampling clock for the SD ADC.



Rad Hard Board Block Diagram

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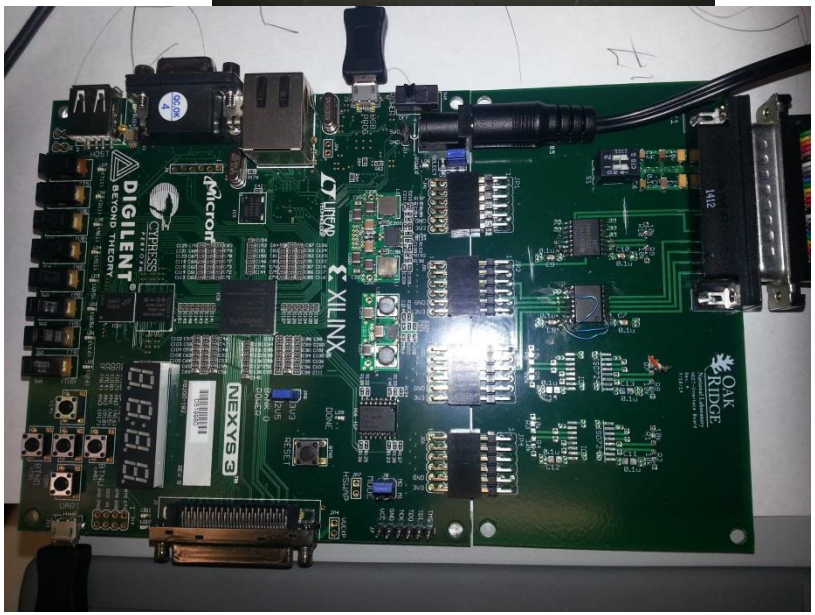
Accomplishments – Sensor Board/ Interface Board

- **Sensor Board implements:**
  - Temperature
  - Pressure
  - GM-tube rad detection

- **Nexys 3/Interface board implements:**
  - Nexys 3 contains a Xilinx Spartan 6 Field-Programmable Gate Array (FPGA)
  - USB communications between computer and rest of system
  - Digital filter for the SD ADCs
  - Counter for the GM-tube rad detector

- **Board status:**
  - Two systems are operational
  - Three more are in fabrication



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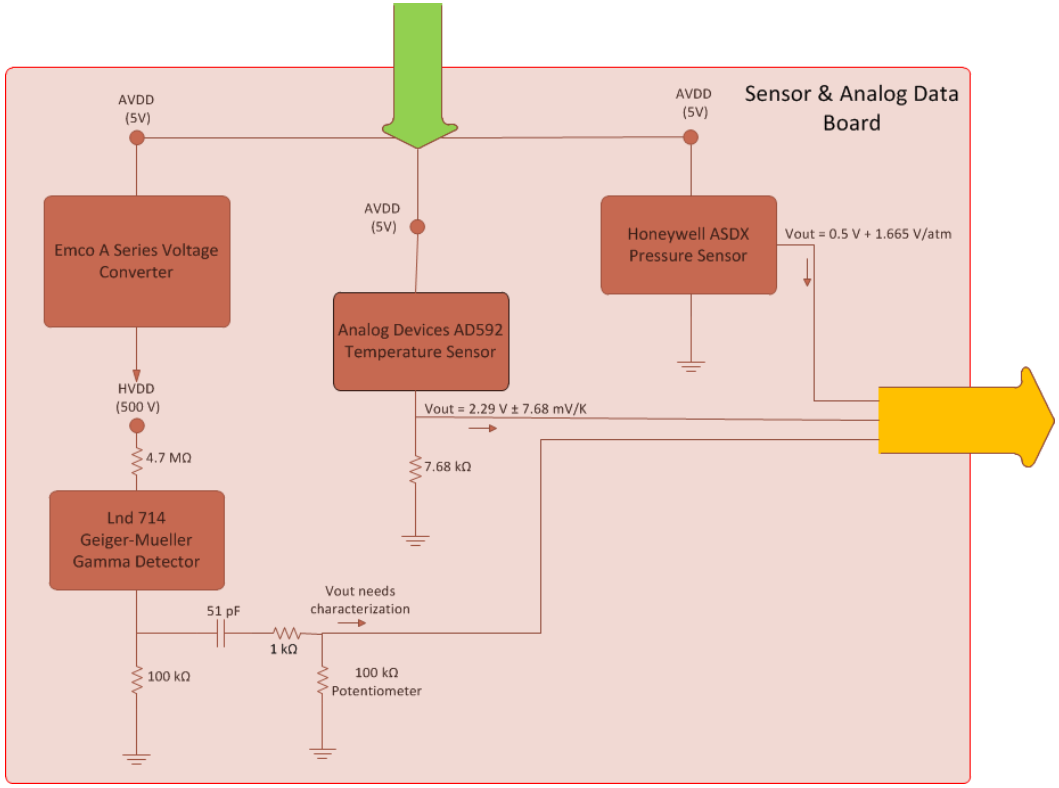
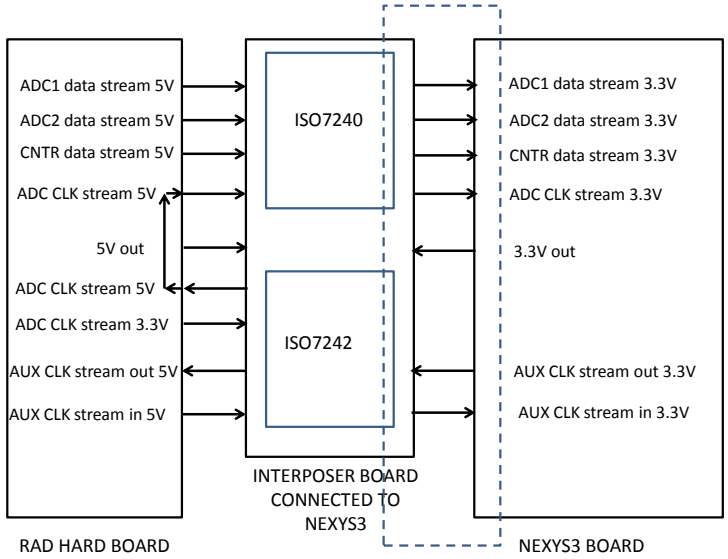
Accomplishments – Sensor Board/ Interface Board



Sensor Board Block Diagram



Interface Board Block Diagram

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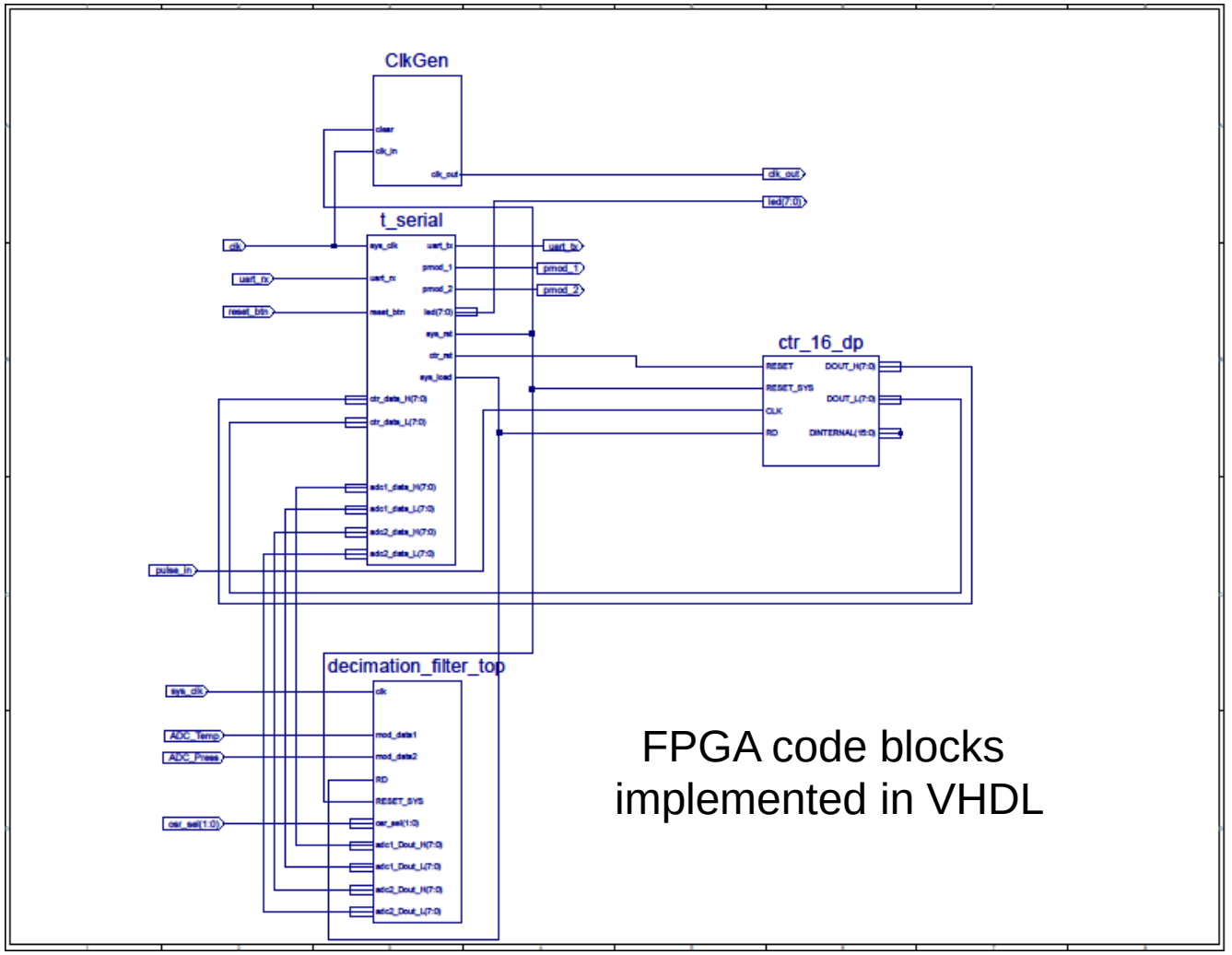
Accomplishments – FPGA Firmware

- **The FPGA program consists primarily of four code blocks**
  - UART (t_serial)
  - Digital filter (decimation_filter_top)
  - Geiger counter (ctr_16_dp)
  - Secondary clock generator (ClkGen)
- **The Spartan 6 has sufficient logic resources.**
- **The Nexys 3 board has**
  - The required USB interface hardware
  - Lots of logic I/O pins for the ADCs and the comparator



FPGA code blocks implemented in VHDL

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Accomplishments – FPGA Firmware

- The command structure between computer and FPGA is very simple
- Each command has one and only one function and an expected data return character
- All transfers are byte-wide
- Commands are combined in strings to implement entire functions

COMMAND	FUNCTION	RETURN CHARACTER
hex 20 (space)	system-wide reset	hex 20 (space)
hex 21 (!)	counter reset	hex 21 (!)
hex 22 (")	system-wide data load	hex 22 (")
hex 30 (0)	counter high-byte load	(data)
hex 31 (1)	counter low-byte load	(data)
hex 32 (2)	adc1(temp) low-byte load	(data)
hex 33 (3)	adc1(temp) high-byte load	(data)
hex 34 (4)	adc2(press) low-byte load	(data)
hex 35 (5)	adc2(press) high-byte load	(data)

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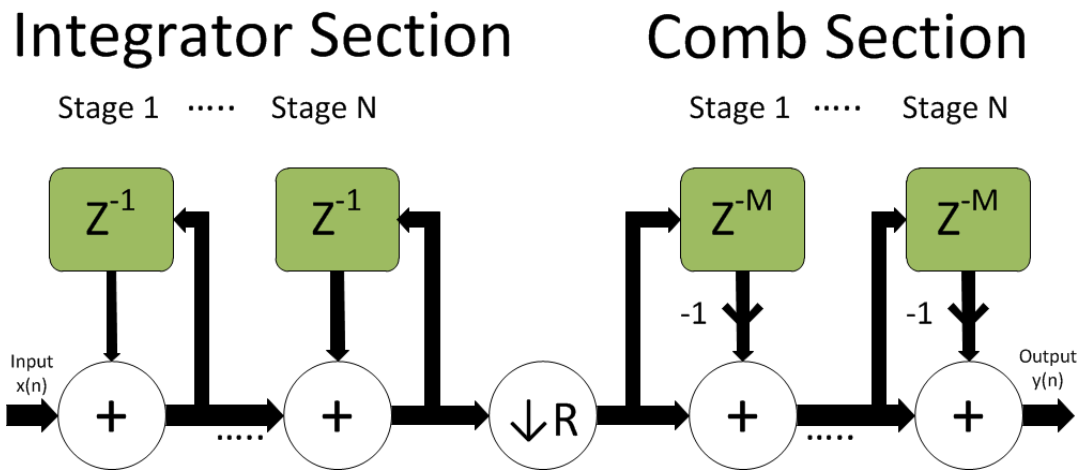
Accomplishments – FPGA Firmware

- The decimation filter is implemented as a third order Cascade, Integrate and Comb (CIC) low-pass filter.
- The purpose of the decimation filter is to filter out the out-of-band digitization noise from the sigma-delta modulator data.
- Input to the filter is a single-bit data with variable pulse density that corresponds to the signal level at the modulator/ADC input.
- In this particular case, the input data represents slowly changing temperature and pressure measurements.
- For all practical purpose the modulator input is considered a DC signal.
- The dynamic range of the filter's output corresponds to more than 13 bits of resolution.



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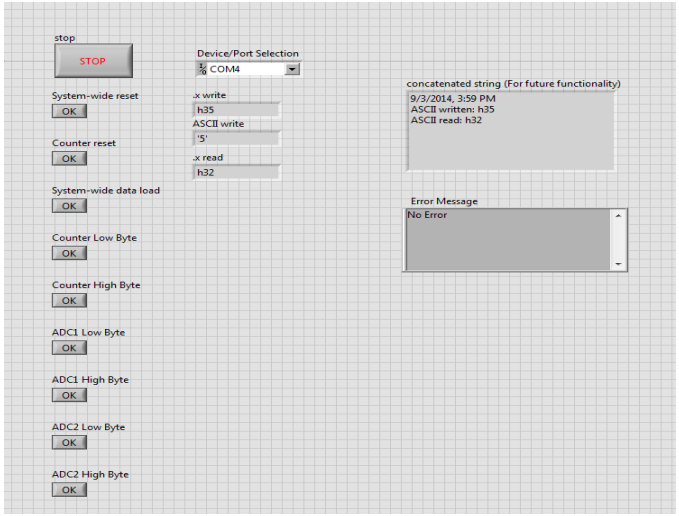
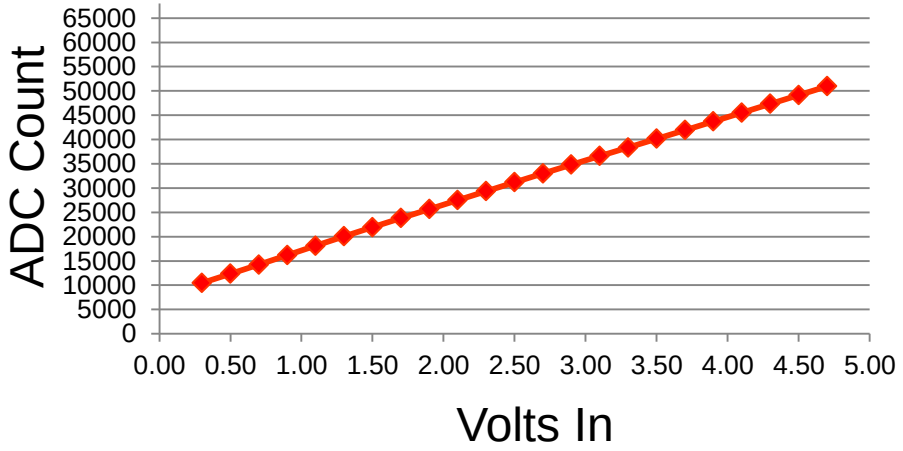
Accomplishments – Software/Testing

- A control program in LabView was written to implement the control/readout functions.
- A histogramming version is in development.
- Typical results are shown at right.



Pressure ADC



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Technology Impact

- Telerobotic technologies that enable remote operation in high dose rate environments have undergone revolutionary improvement over the past few decades. However, much of this technology cannot be employed in nuclear power environments due the radiation sensitivity of the electronics and the organic insulator materials currently in use.

- As the recent accident at Fukushima Daiichi so vividly demonstrated, telerobotic technologies capable of withstanding high radiation environments need to be readily available to enable operations, repair, and recovery under severe accident scenarios where human entry is extremely dangerous or not possible.

- The proposed work will produce a prototype rad-hard data acquisition system that will be constructed and tested to demonstrate functionality and rad-hardness of the identified pre-commercial or commercial technology, as applied to a nuclear reactor environment.

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Conclusion

- We are evaluating new electronic technologies, in particular rad-hard analog array ASICs, that are commercial or near commercial for reactor and cleanup applications.

- The Triad rad-hard VCA is a proven via-configurable analog concept that should be of great interest to the nuclear community in that it:
  - Can be manufactured commercially.
  - Allows analog functions to be designed like a digital array thus simplifying development.

- The extreme radiation environment of both reactors after accident and the various cleanup operations will need the hardness of these types of circuits for long loiter times.

- We would like to be able to transition rad-hard work after this project ends into a real robot for cleanup with our partner at PNNL (Sharon Bailey).