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DOE SBIR HV DC Link Grant #SC0008240

15 kV Phase Leg Power Modules with SiC MIDSJT Devices

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GeneSiC
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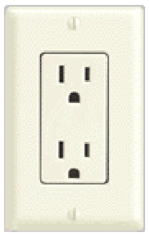
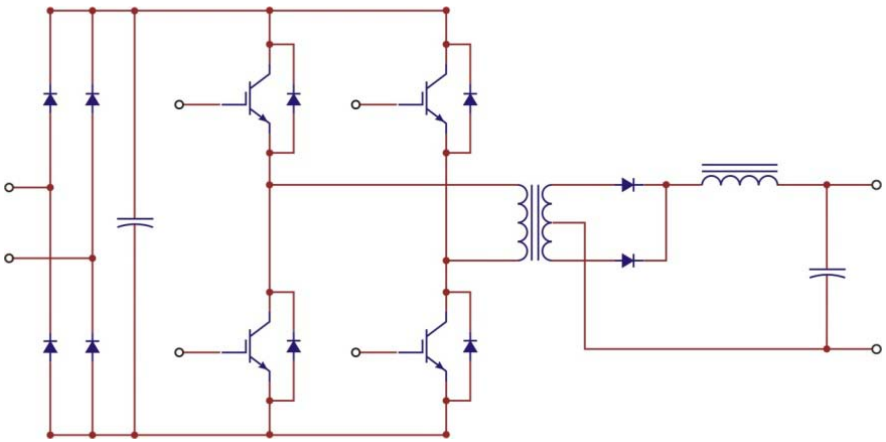
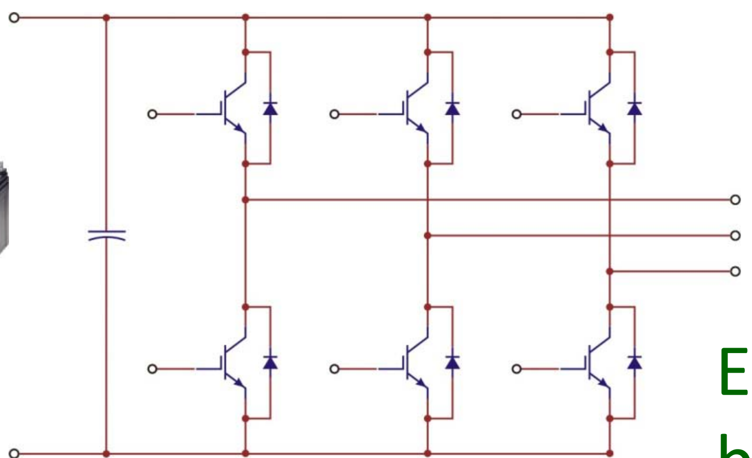
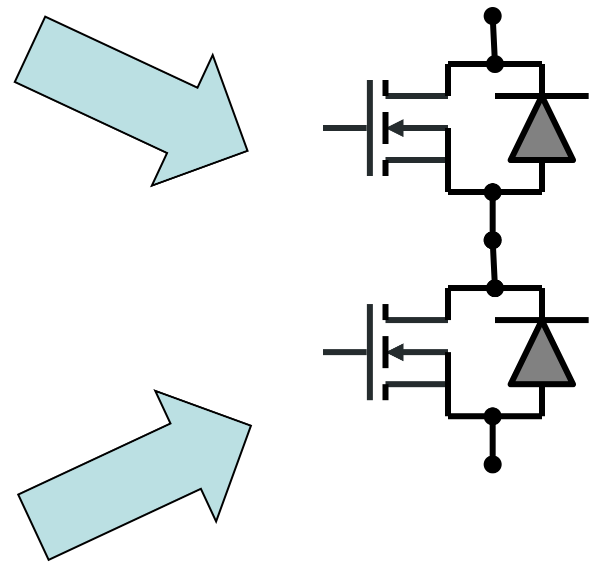
Phase Leg forms fundamental building block for AC/DC AND DC/AC Conversion



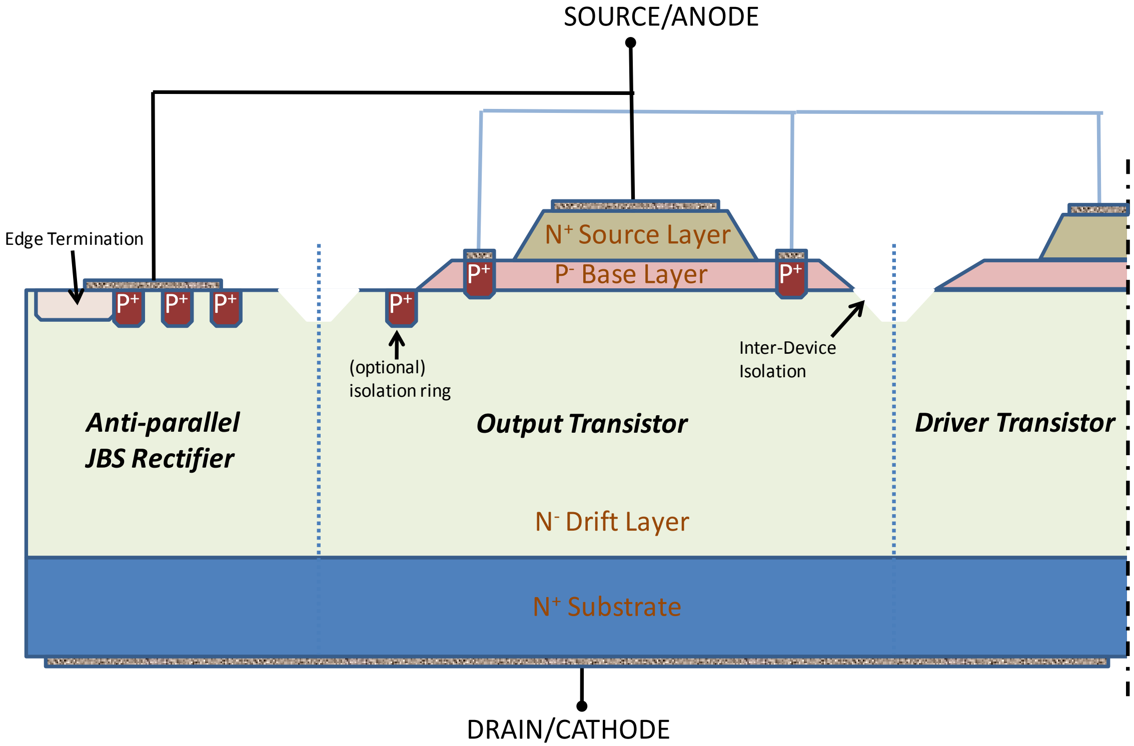


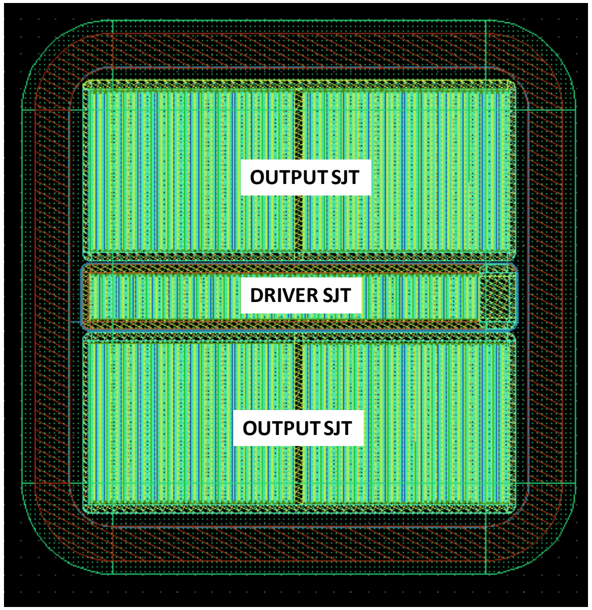




Each switch and diode must be capable of 15 kV/10KHz

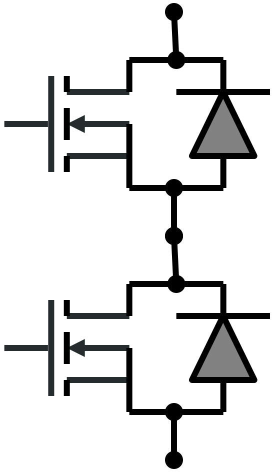
Novel Single-chip Monolithic Integrated Diode Super Junction Transistor (MIDSJT)

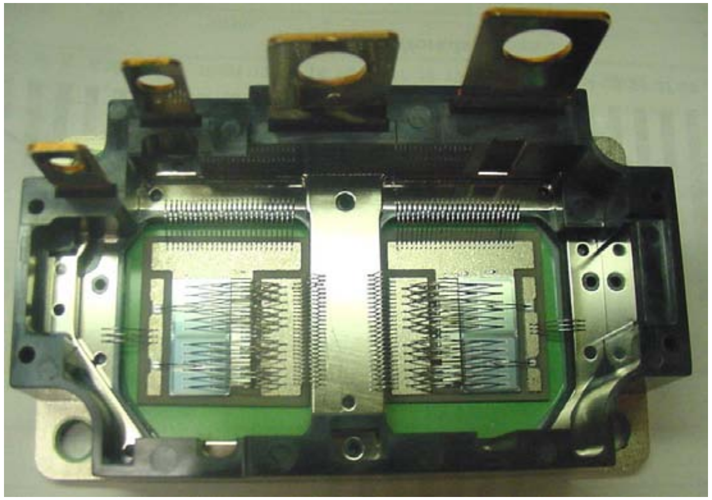




- If achieved it will be the first time a 15 kV integrated circuit is demonstrated
- Universal applicability towards all grid-connected (15 kV/10 A) power electronics

Goals for this Project: Phase Leg using Single Chip MIDSJT





Pre-Phase I

- 10 kV SJTs demo
- 10 kV JBS diodes demo

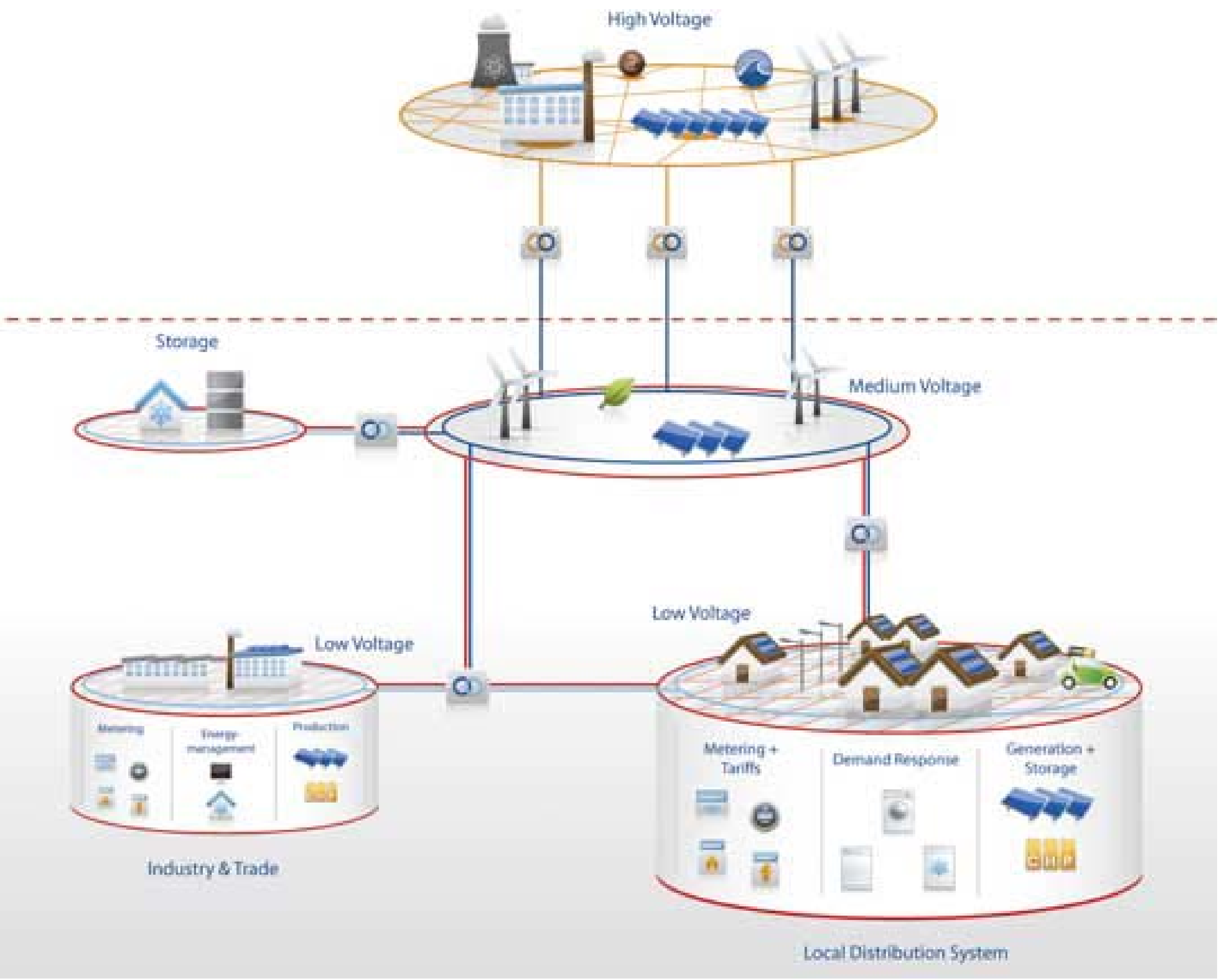
Phase I (7/12-4/13)

- Prove Integrated SJT/Diode chip at 1200 V
- Design 10 kV Integrated Devices

Phase II (8/13-8/15)

- 15 kV Integrated SJT/Diodes
- >10 A
- Optimized Packaging

Energy Storage at Medium Voltages

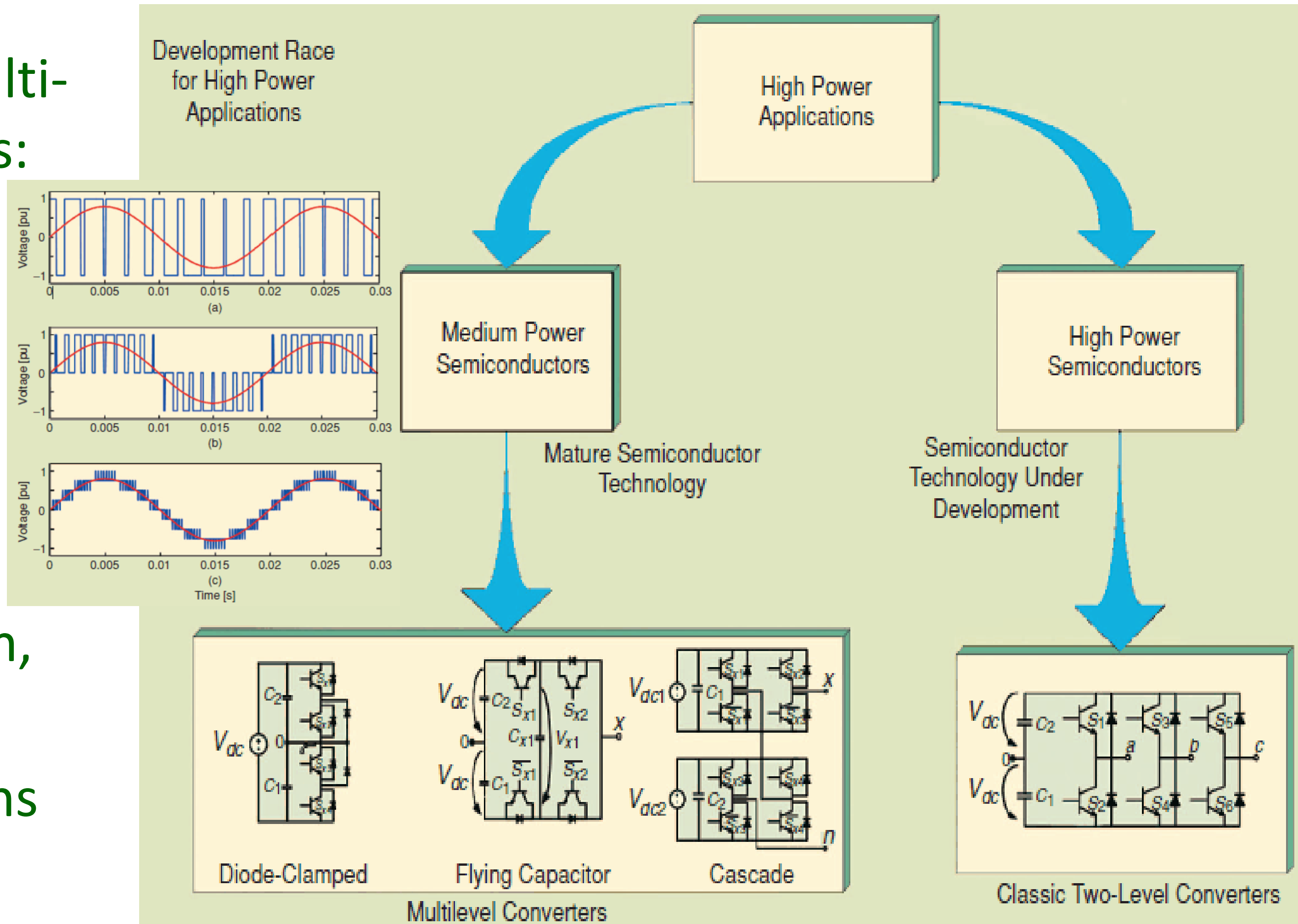


- Many storage opportunities exist at medium voltages
- 13.8 kV and 4.16 kV are commonly used voltages
- Silicon Carbide high voltage devices play a pivotal role at these voltages

Multilevel vs Two-Level Converters

Trade-Offs in Multi-level converters:

- Efficiency
- Robustness
- Modularity
- Design Implementation, Complexity
- Control concerns
- Fault Tolerance

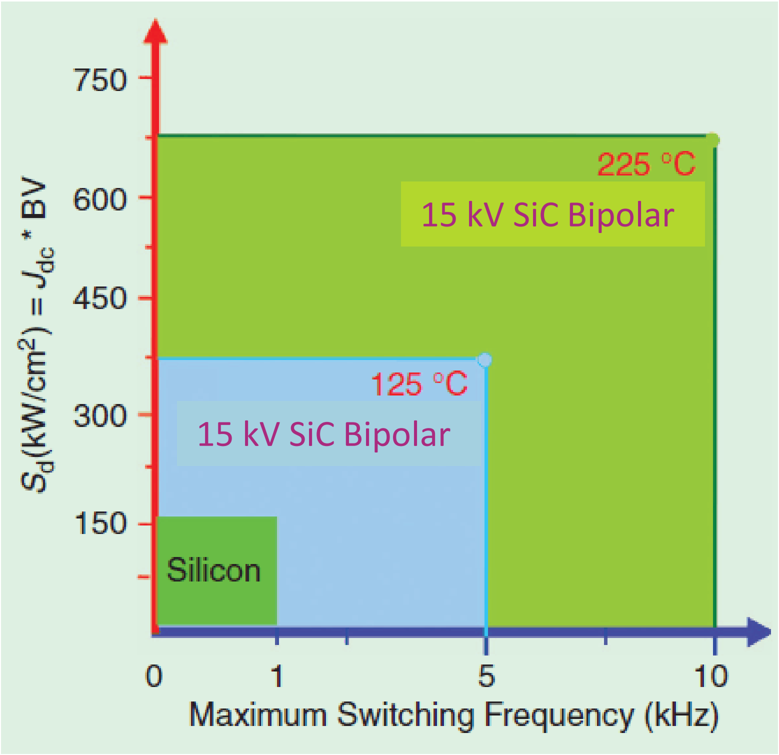


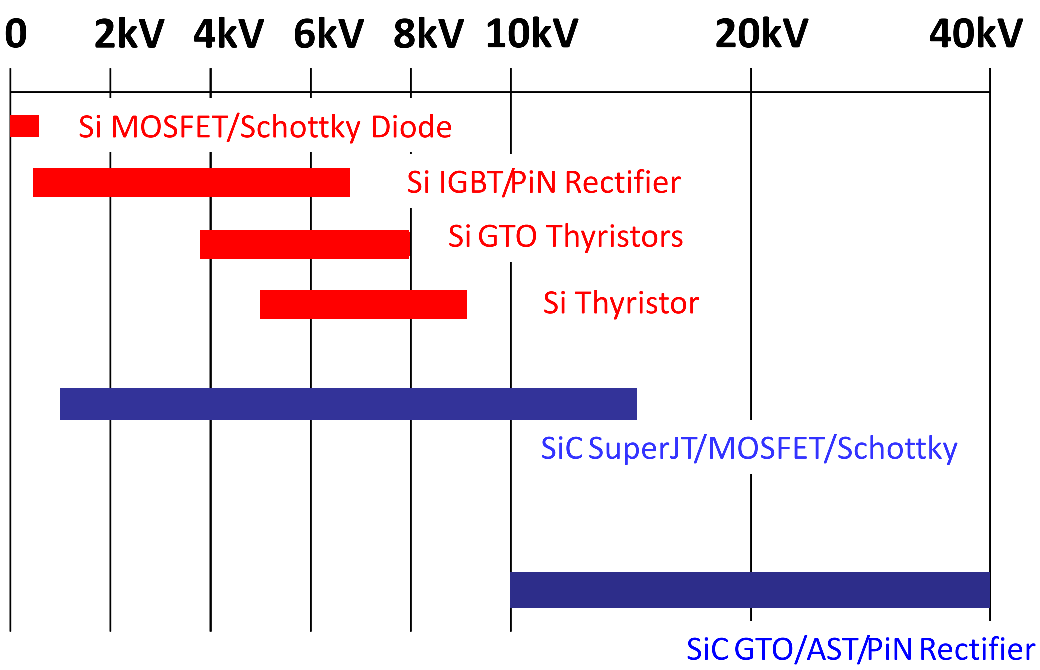
From: Franquelo et al.

Why SiC Power Devices at Medium Voltages?

Properties SiC vs Si	Performance of SiC Devices	Impact on Power Circuits
Breakdown Field (**10X**)	Lower On-state Voltage drop (**2-3X**)	Higher Efficiency of circuits
Smaller Epitaxial Layers (**10-20X**)	Faster Switching speeds (**100-1000X**)	Compact circuits
Higher Thermal Conductivity (**3.3-4.5 W/cmK vs 1.5 W/cmK**)	Higher Chip Temperatures (**250-300°C instead of 125°C**)	Higher pulsed power Higher continuous current densities,
Melting Point **(2X)**	High Temperature Operation (**3X**)	Simple Heat Sink
Bandgap **(3X)** (**10^{16}X** smaller n_i)	High Intrinsic Adiabatic Pulsed Current Level (**3-10X?**)	Higher Current Capability

Ratings of SiC and Si Devices



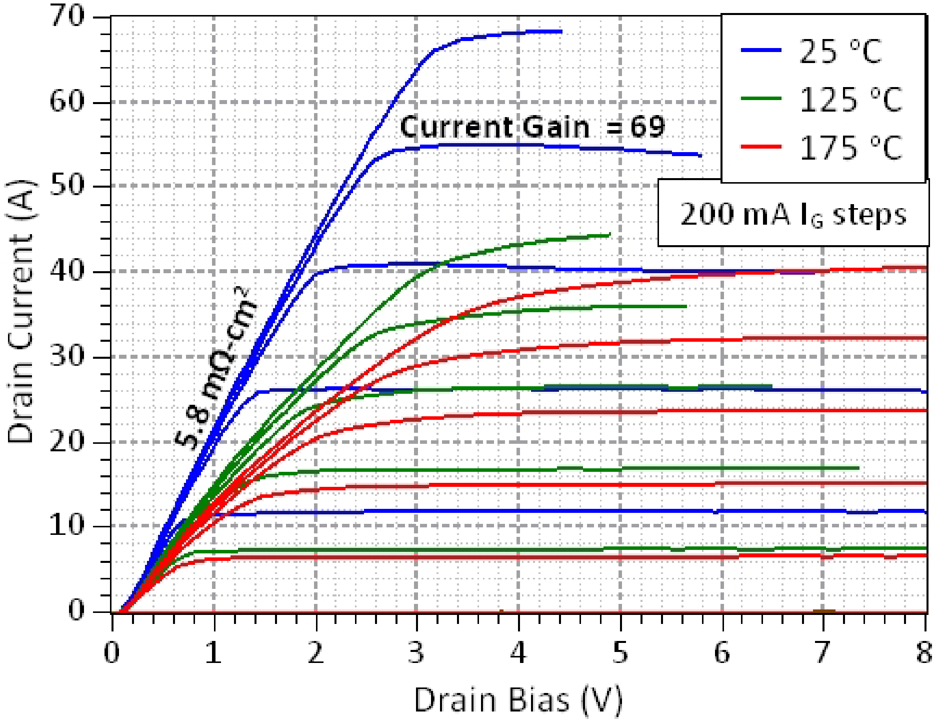


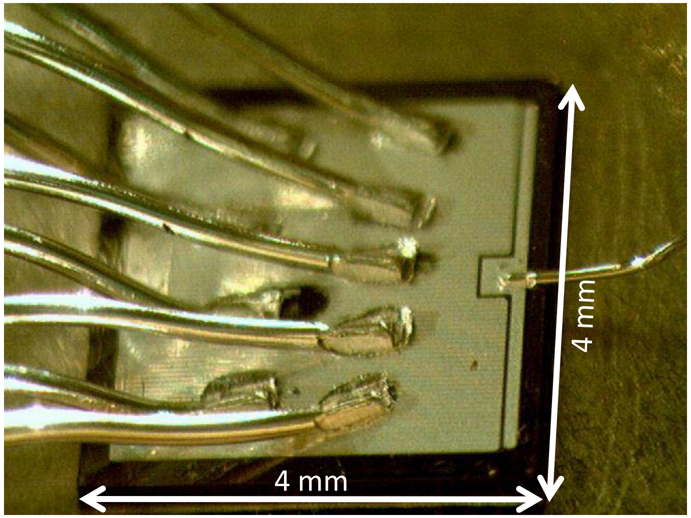
- Maximum Voltage and Current Ratings of UHV SiC Bipolar Devices significantly higher than theoretical capability of Si
- Further SiC offers unprecedented margins from failures

15 kV SiC Switch Comparisons

	MOSFET	JFET-ON	JFET-OFF	BJT	SJT
Gate Control	+20V/0V No Current	+0V/-20V Low Current	+3/0V Current Gain	+3V/0V Current Gain	+3V/0V Current Gain
Current Gain	Infinite	>1000	~50 (at rated current)	~30 (at rated current)	>100 (Target at rated current)
Current Rating	Very low	High	Low	High	High
Fabrication Cost	Very High	Medium	High	Low	Low
Switching Speed	Medium (Gate Cap)	High	Low/Medium (Gate-Source Cap)	Very low (Minority injection)	High (Low cap, No Minority)
High Temperature	Very Poor	Very Good	Medium	Very Good	Very Good

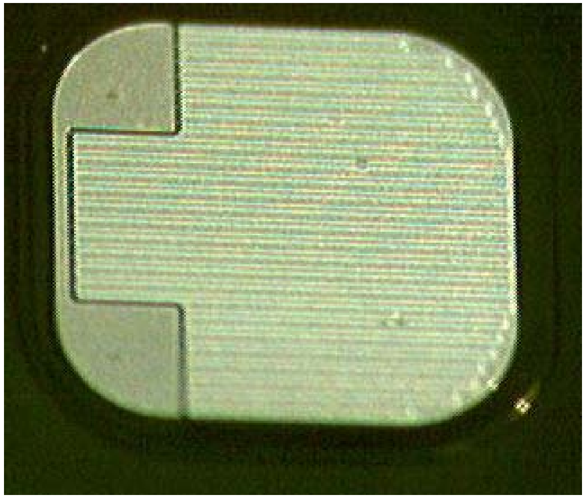
High Current SJTs – output characteristics

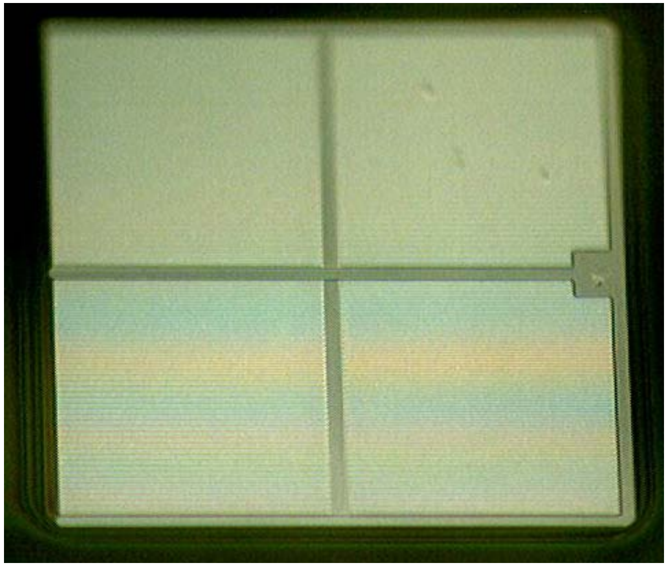


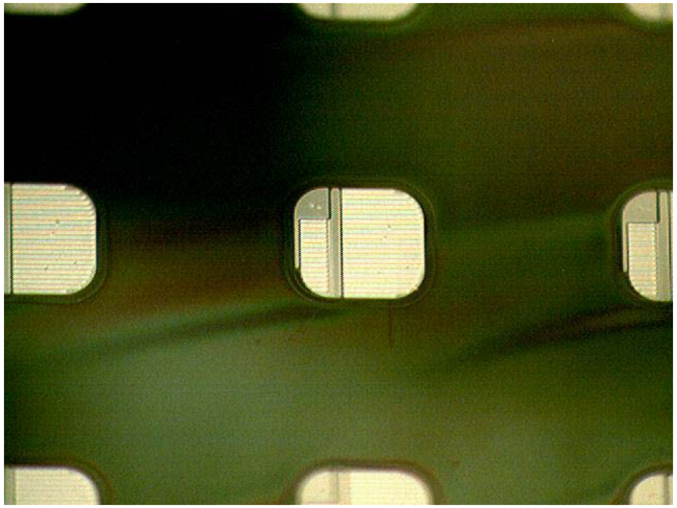


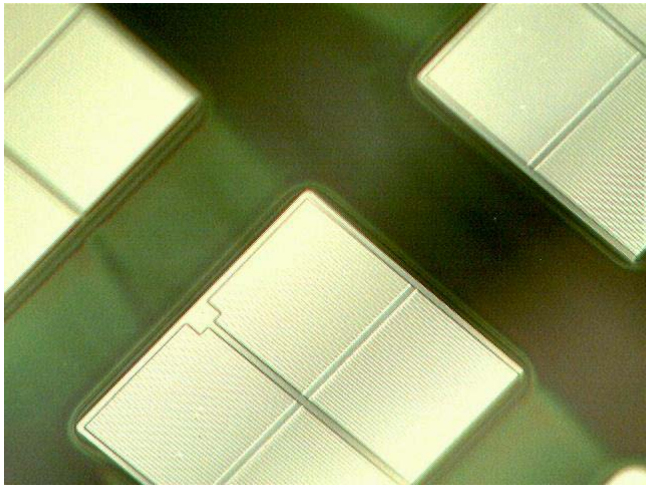
- Low on-resistance of achieved in a 1200 V SJT
- High Current gain recorded at Drain Current of 55 A at 25 ºC.
- Positive temperature co-efficient of on-resistance exhibited, which is desirable for paralleling multiple devices.

Photographs of fabricated 10 kV SJTs

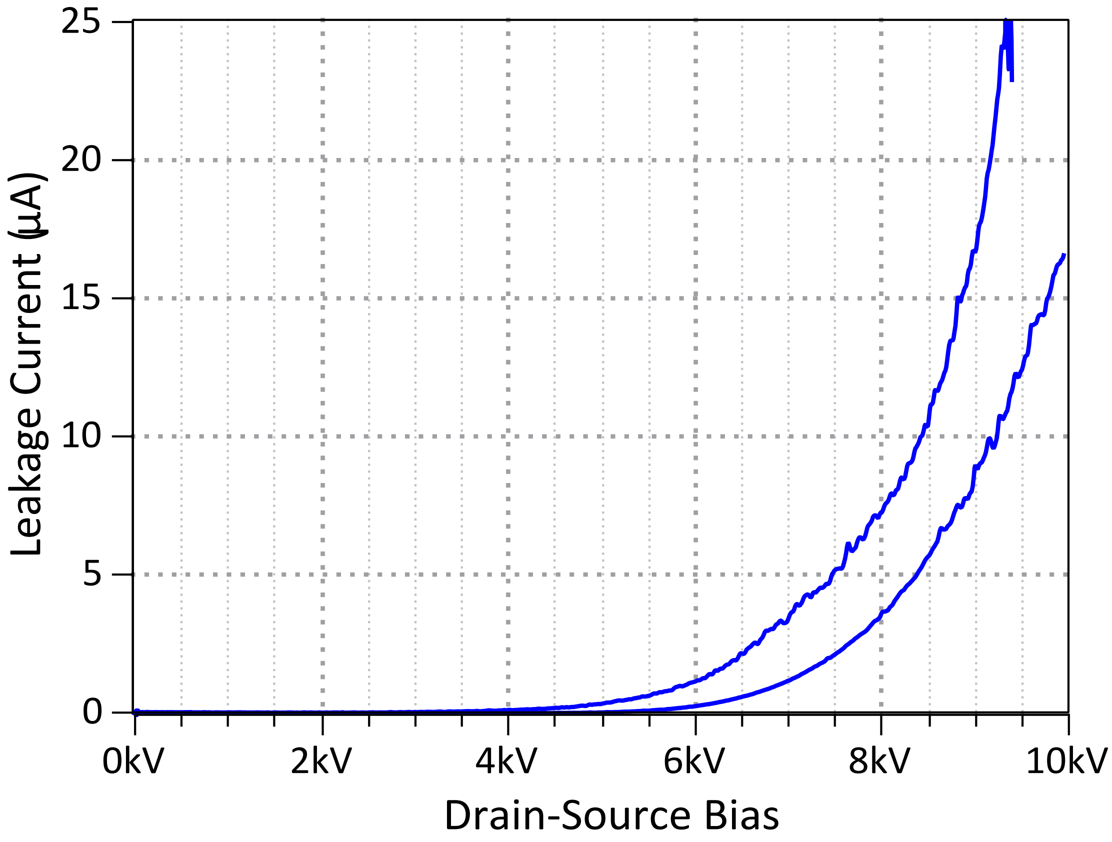






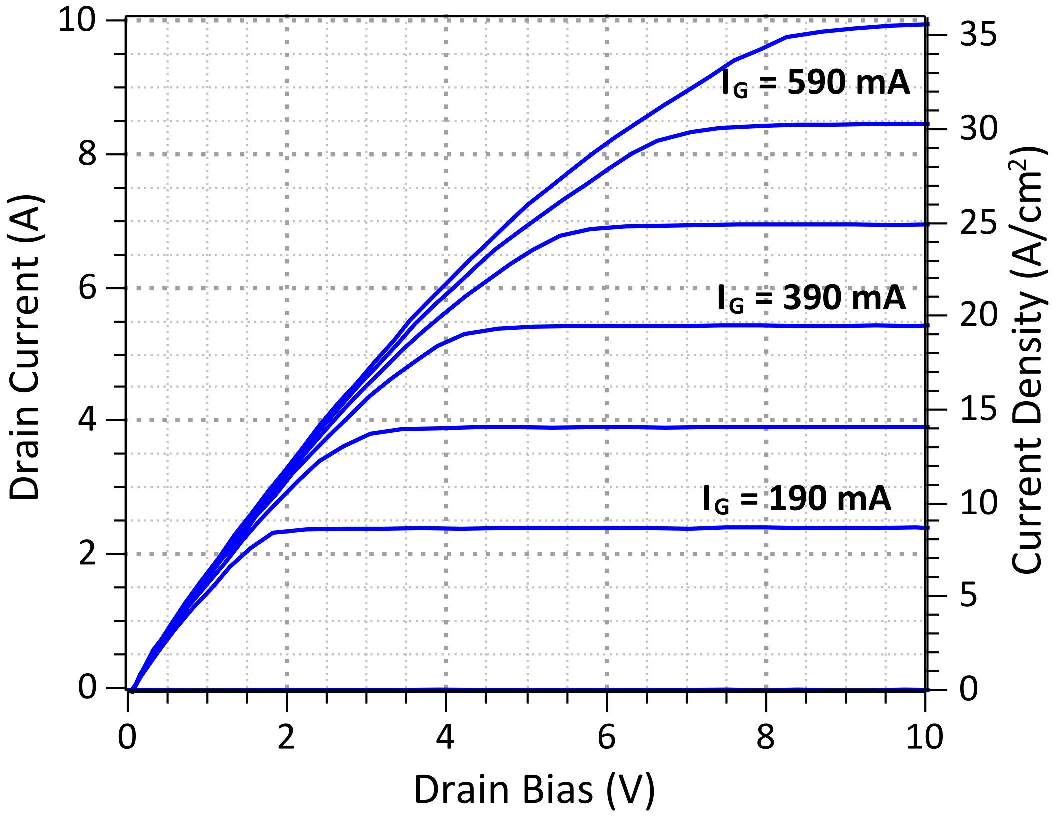


On-wafer characterization – Blocking Voltage (BV) characteristics



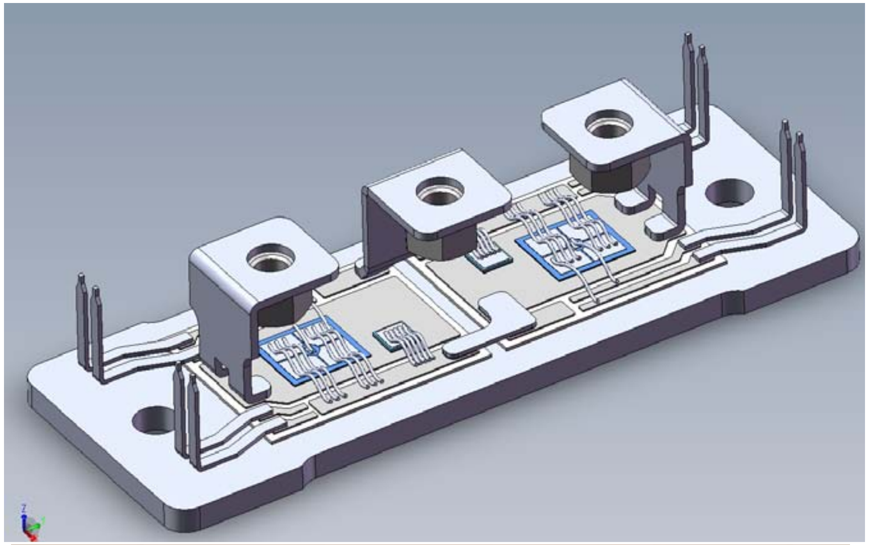
- BV as high as 10kV recorded on 0.025 cm^2
- BV as high as ~9kV recorded on 0.28 cm^2 SJTs

Output characteristics of 0.28 cm^2 on 10 kV SJTs

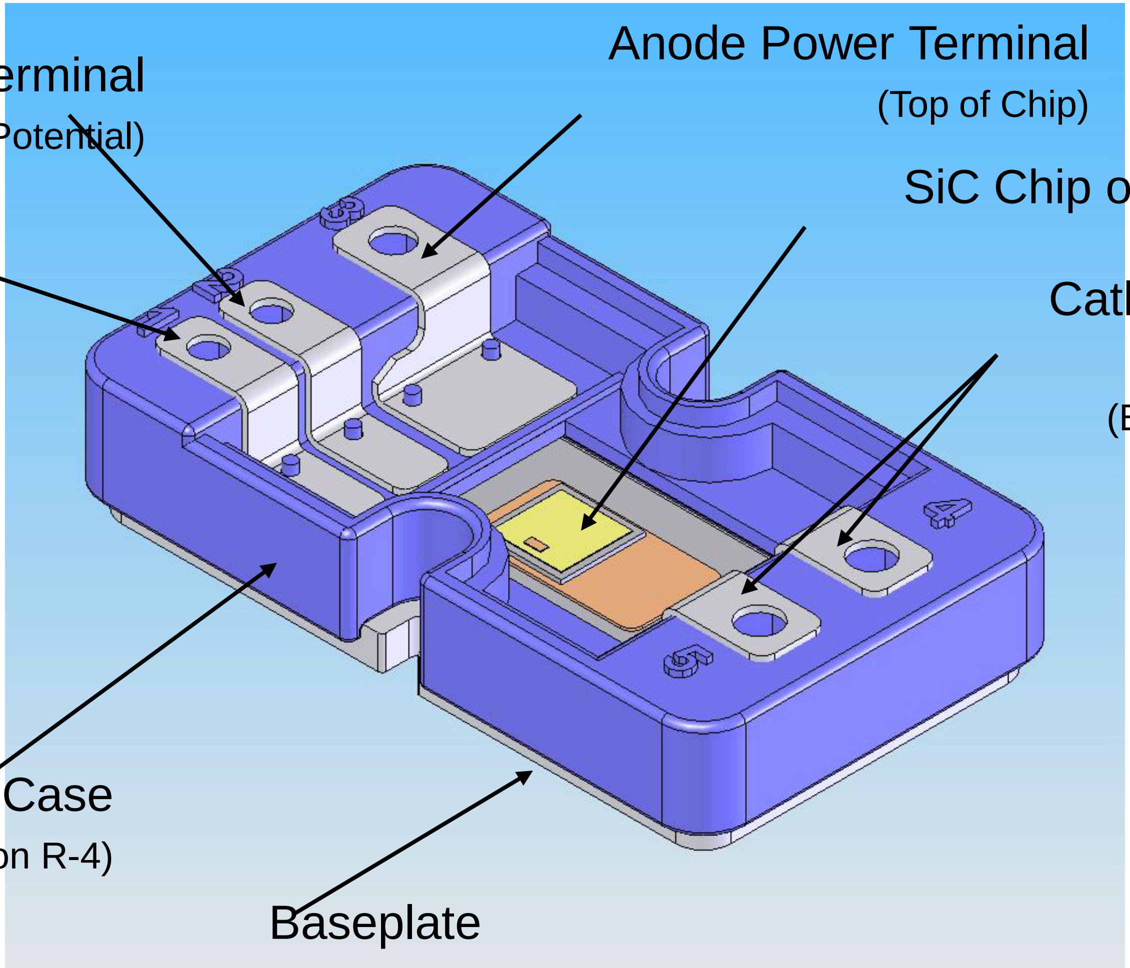


- Excellent Gate-Source shorting yield observed for 0.28 cm^2 SJTs

GeneSiC's commercial Phase Leg Packaging



Module Configuration



Status and Future Efforts

- Current Status
  - Fabrication steps of 1200 V MIDSJT being completed as proof of concept
  - Design of Silicon Carbide Monolithically integrated diode/Super Junction Transistor (MIDSJT) being conducted
- Future Efforts in Phase I
  - Characterize devices from present batch and study MIDSJT concept
  - Complete layout, fabrication and characterization plan for 15 kV/10 A devices

Grant Details

- Principal Investigator: Dr. Siddarth Sundaresan
- Program Manager: Dr. Ranbir Singh
- Grantee:

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