Accelerated Testing and Modeling of Utility-Scale Power Electronic Devices

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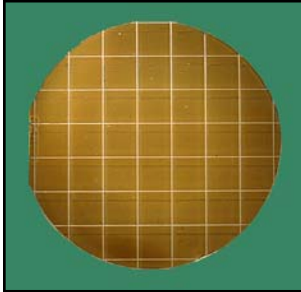
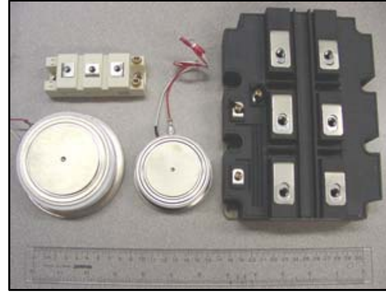
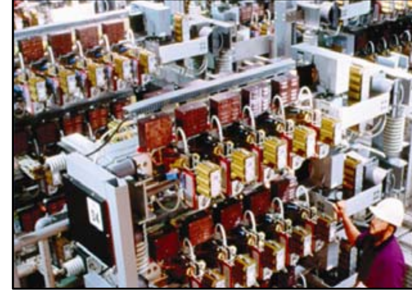
There are Power Electronics Research Needs at Many Levels: Our Project Addresses Two







Applied Materials Research

Power Electronic Module Development

Next Generation Equipment

System Reliability

This Project's Work Involves These Two Sectors

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The Following Will Be Presented

- Limitations of power electronic devices (PEDs)
- What is this project doing to help overcome them?
- Progress since project’s inception (Apr08)
- Summary
- Future Work

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Existing PED Limitations for Medium and High Voltage Converters Must Be Overcome for Utility Applications

Today:	Where They Need To Be:
< 5 kHz	$\geq$ 20 kHz
Si-based thyristors	SiC-based thyristors & SiC-based insulated gate bipolar transistors (IGBTs)
6 kV devices	20 kV devices
125° C limit	300° C capability (including packaging)
Designs are custom	Application ready & modular
Small suite of accelerated test methods for thyristors	Developmental PEDs need to be “vetted” by effective and relevant accelerated test methods that fully harvest statistical results

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This Project's Approach Has Two Parts

1. **Develop accelerated tests for thyristors, gate turn-off thyristors (GTOs), and integrated gate commutated thyristors (IGCTs) employing existing capabilities at ORNL**
    - **High current power supply (46 V – 2400 A)**
    - **High voltage power supply (25 kV – 4 A)**

2. **Model stress states in thyristor subcomponents and make recommendations that will lessen their magnitude (& improve reliability) and consider alternative material constituents in PE devices**

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Toward Accelerated Testing…

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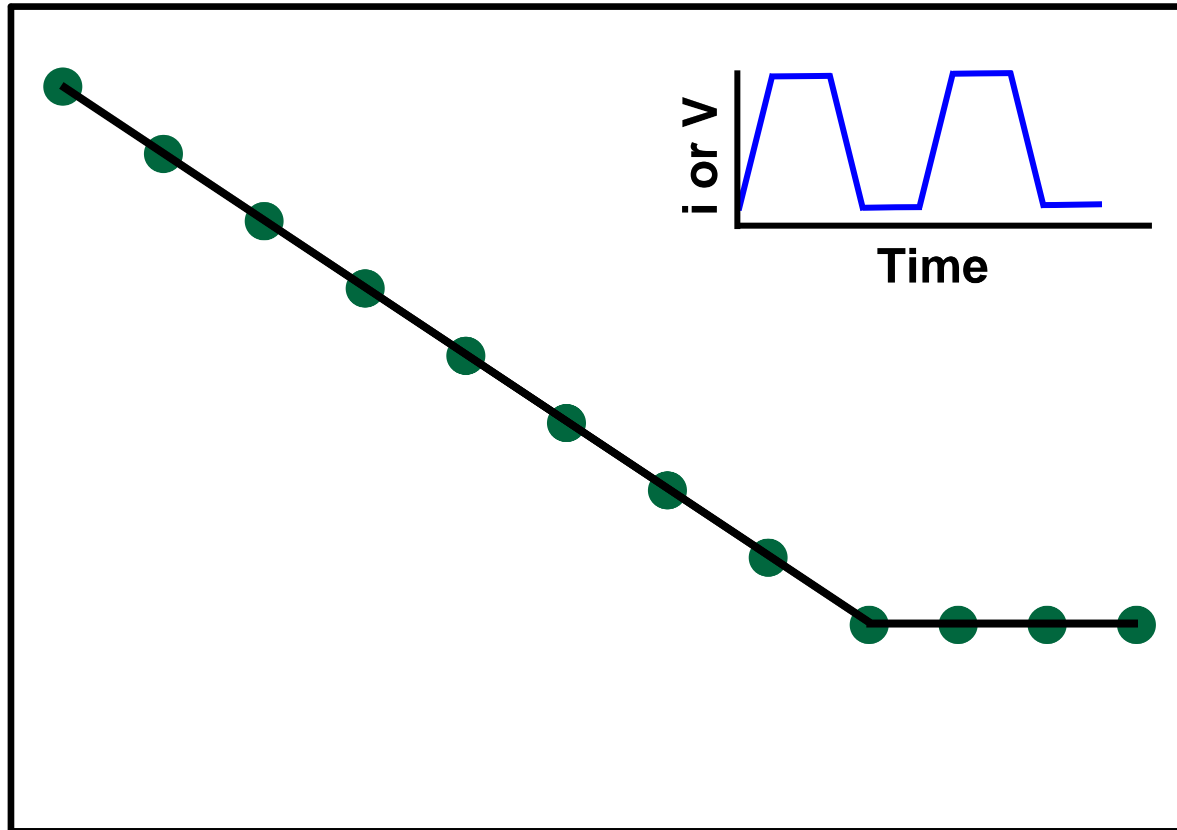
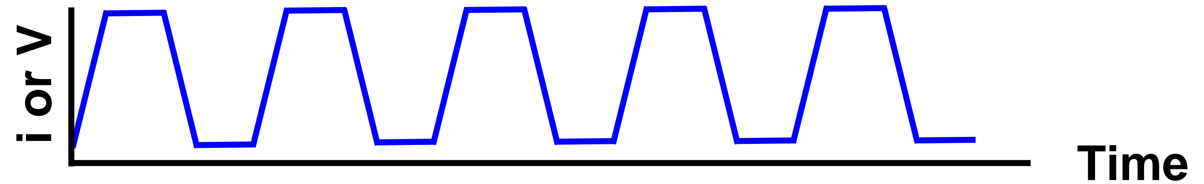
A Characteristic Lifetime or “Fatigue” Response Can Be Determined for Any Given PE Device

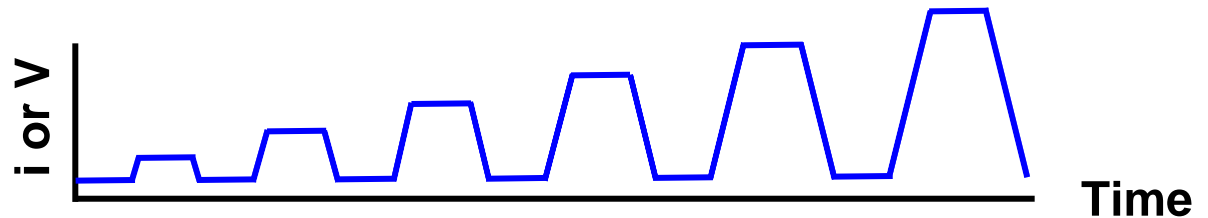


Special Software Is Being Developed to Drive the Power Supplies and PE Devices With Waveforms that Will Hasten Mortality (Using Either i or V)

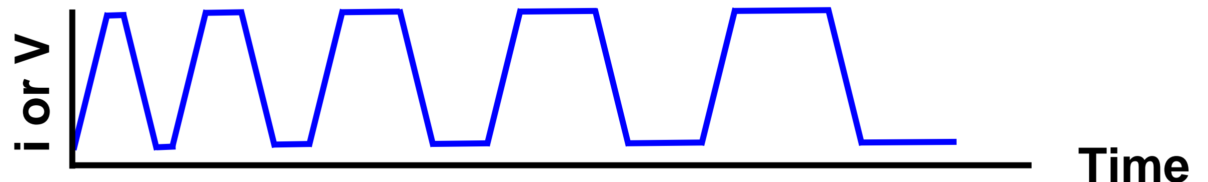
Constant Amplitude & Dwell



Constant Dwell & Constant Rate of Amplitude Increase



Constant Amplitude & Constant Rate of Dwell Increase



Approach adapted from the accelerated testing of mechanical fatigue

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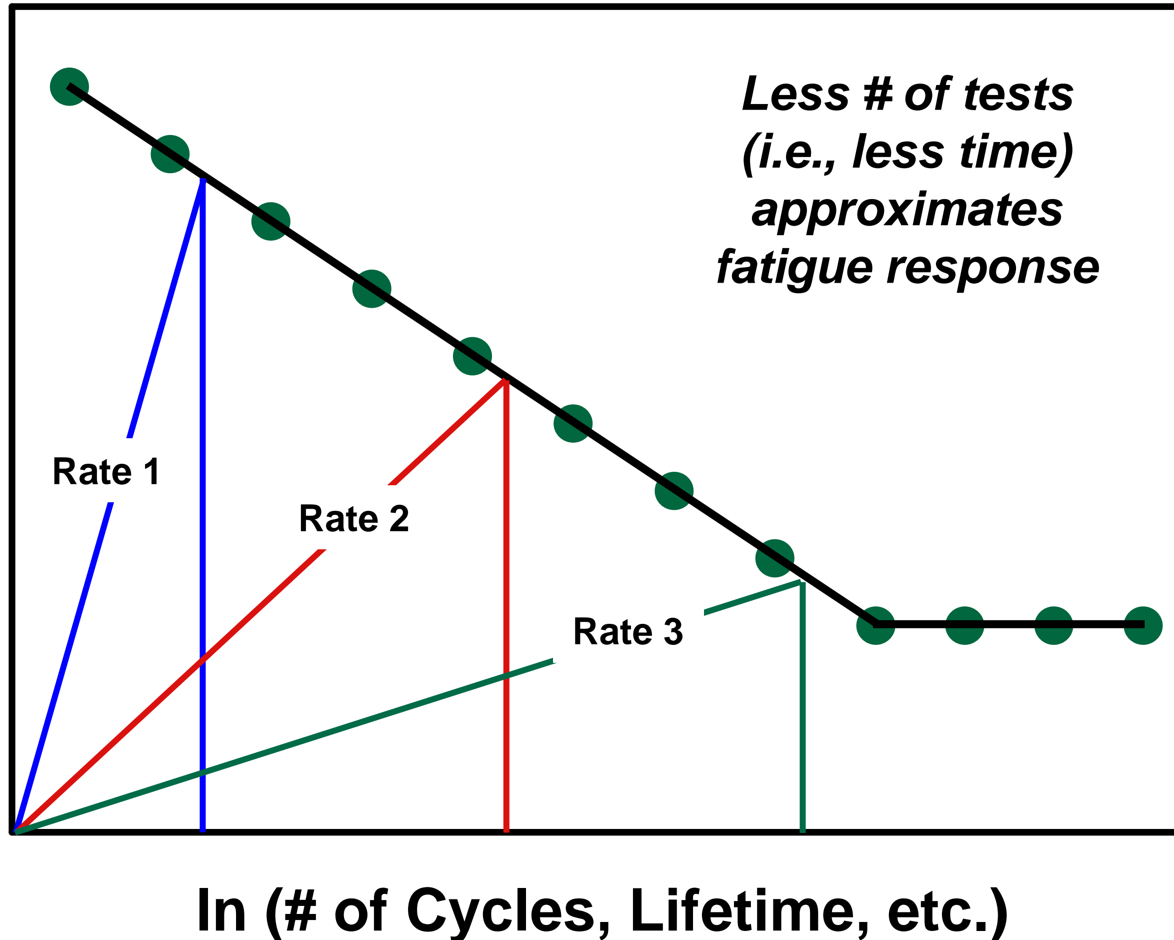
Dynamic Changes in the Waveforms Will Be Sought to Accelerate Lifetime



Some Dependent Parameters:

- Breakdown voltage
- Forward voltage and resistance
- Leakage current
- Switch times

Approach adapted from the accelerated testing of mechanical fatigue

Thermomechanical Modeling of Thyristor…

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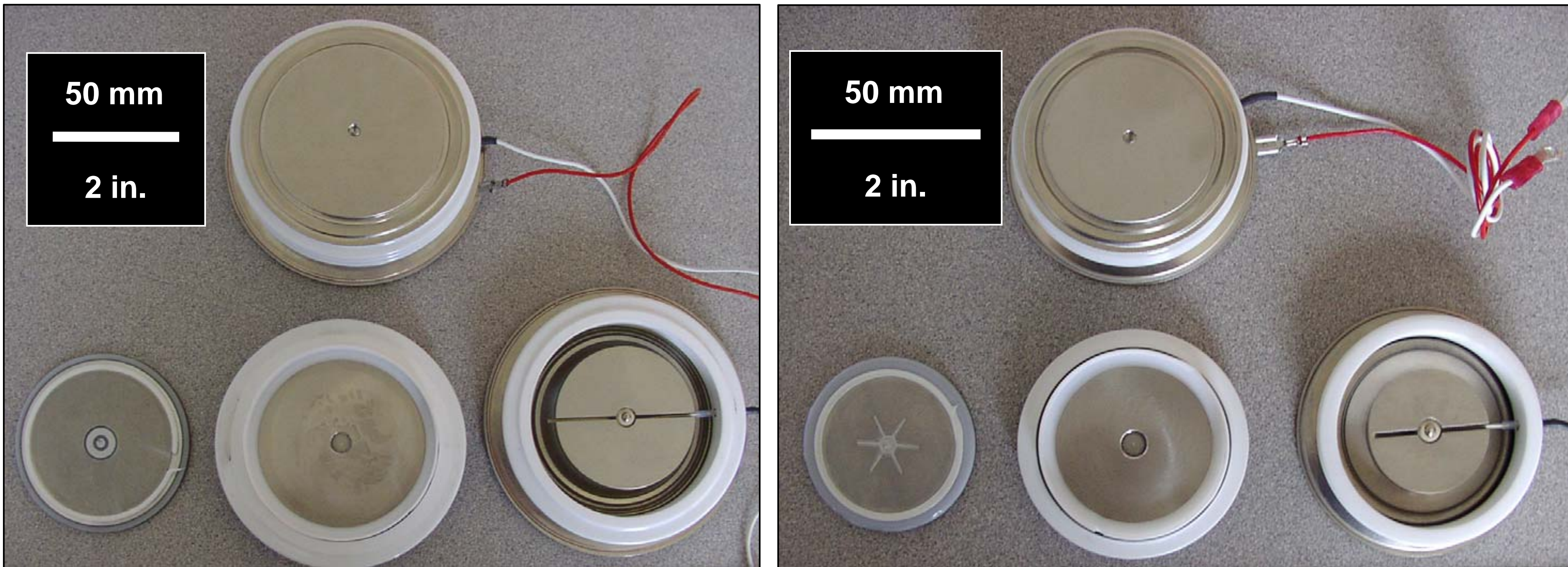
Examples of Dissected Thyristors

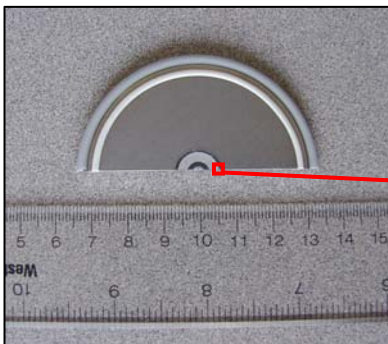
Such dissection enables cross-sectioning exams…

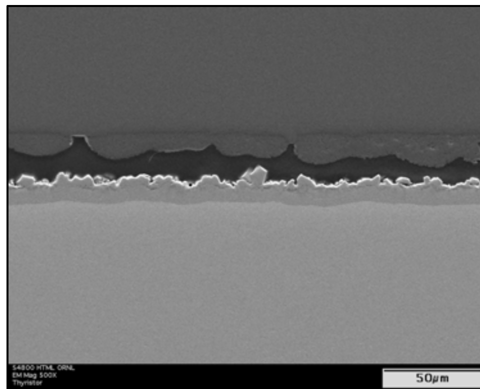


A Preliminary Observation:
The cathode tends to be very weakly bonded to the Si wafer

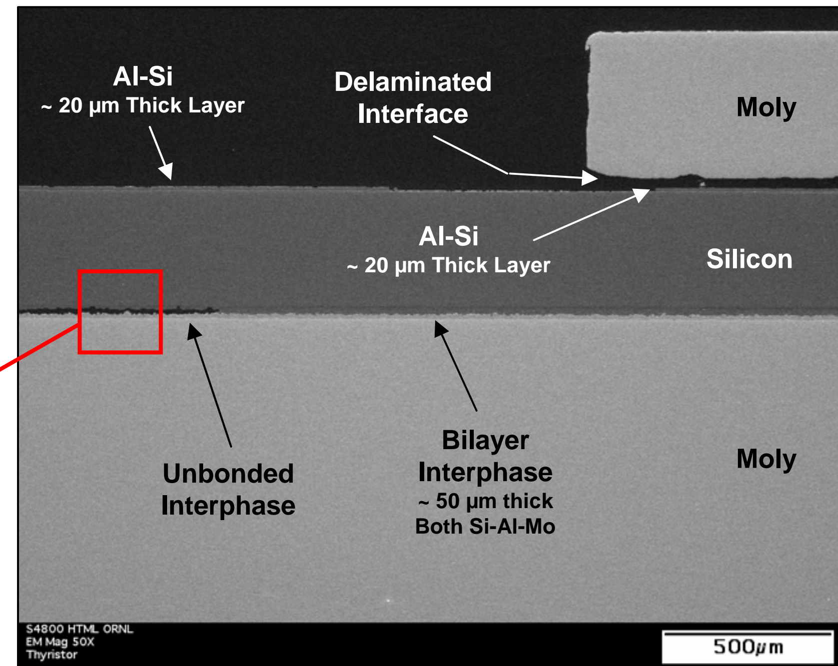
Materials and Architectures Comprising the Thyristor Are Being Investigated to Ultimately Improve Thermal Management and Reliability

Sectioned Thyristor (top view)





Magnified Side View



SEM Images taken by ORNL's H. -T. Lin

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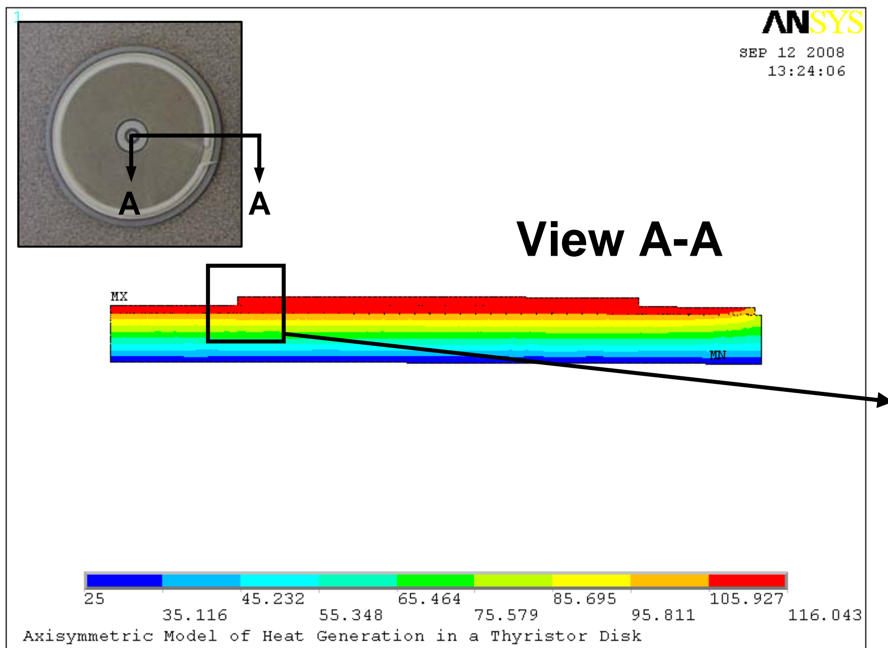
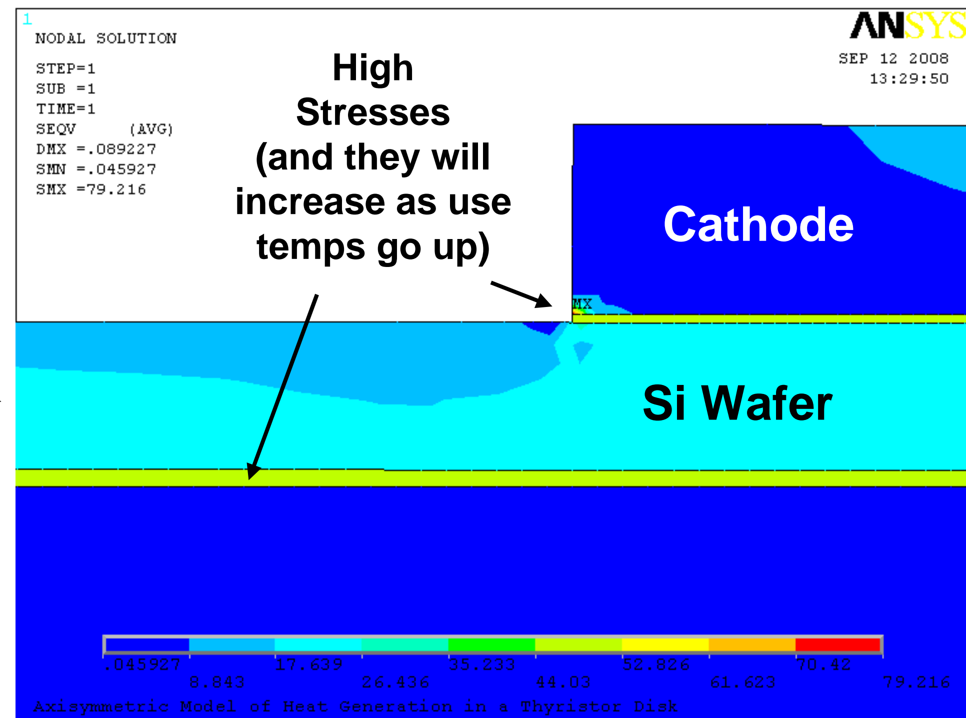
Thermomechanical FEA Shows High Stresses Exist in Metallic Layers Bound to the Si Wafer

Axisymmetric FEA Model (Temperature Profile)



Von Mises Stress Field Caused by Induced Temperature Field, CTE Mismatches, and Residual Stresses



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Summary of FY08 Milestones & Accomplishments

- **Milestones**

  1. **Document the architectural and material reference state of a PED by cross-sectioning a commercially available 1600V/1800A thyristor, quantifying the dimensions of its cathode, gate, wafer, and anode, and identifying material constituents *[May08 – completed]***

  2. **Develop and adapt test algorithms and requirements for accelerated testing of thyristors *[Dec08 – on schedule]***

- **Accomplishments**

  1. **Sectioned and characterized architecture of 1600V/1800A thyristor**

  2. **Adapting accelerated mechanical fatigue test strategies to that for PEDs**

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Other Recent Relevant Progress

- **Discussed waveform needs with software developer and ordered the software**
- **Identified high voltage power supply. High current power supply identified earlier.**
- **Identified L. Reddy as a UT EE graduate student to assist in the project**
- **Completed a literature survey on accelerated test methods of PEDs with focus on thyristors (L. Reddy)**
- **Developed mechanical test method to measure adhesion strength of the interface between thyristor cathode and silicon wafer**
- **Developed test method (anticlastic bend test) to measure strength of silicon for use in FEA models**

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Summary

- **Accelerated testing is being pursued by controllably overdriving current or voltage and monitoring breakdown voltage, forward voltage and resistance, leakage current, and changes in switch times**
- **Thyristors were dissected to enable FEA model creation and thermomechanical analysis**
- **Thermomechanical analysis will enable the recommendation of alternative PED subcomponents that will reduce stress and increase reliability without compromising electronic function.**

Improved thermal management and higher-temperature capabilities of utility-scale PEDs will be a consequence of this project's work

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Future Work

- **Establish high-current and high-voltage accelerated test facilities at ORNL**
- **Refine FEA thermomechanical model of PED (thyristor) and begin substituting in alternative subcomponent materials**
- **Establish and build relationships with PED manufacturers**
- **Quantify adhesion strength of interface between thyristor cathode and Si wafer**
- **Adapt FEA coupling effect of electric field on thermomechanical response of PEDs**
- **Measure anticlastic bend strength of both Si and SiC die for use in FEA models**