Power Electronics Packaging

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Oak Ridge National Laboratory

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Project ID: APE049

This presentation does not contain any proprietary, confidential, or otherwise restricted information

Overview

Timeline

- Start – FY13
- Finish – FY15
- 50% complete

Budget

- Total project funding
  - DOE share – 100%

- Funding for FY14: $650K
- Funding for FY13: $700K

Barriers

- Existing standard automotive inverter designs with Si will likely not meet the DOE APEEM 2020 cost, efficiency and density targets.
- State of the art (SOA) power module and inverter/converter packaging technologies have limitations in electrical, thermal, and thermo-mechanical performance, as well as manufacturability.

Targets Addressed

- 40% cost reduction and 60% power density increase of the power module, to meet the DOE power electronics 2020 targets

Partners

Industry: CREE, Infineon, Remtec, Cool Innovations, Fralock, USDRIVE Members, etc.

NREL Kevin Bennion

UTK: Fred Wang, Leon Tolbert

ORNL Team Members: Lixin Tang, Randy Wiles, Andy Wereszczak, Steven Campbell

Project Objective

- **Overall Objective**

➢ **Develop advanced packaging technologies for wide bandgap (WBG) power electronics:** Advancing automotive power modules and power converters in electrical performance, cooling capability, thermo-mechanical performance, and manufacturability, resulting in comprehensive improvement in cost-effectiveness, efficiency, reliability and power density of electric drive systems.

➢ **Provide packaging support for other VTO APEEM projects for systemic research:** Fabrication of customer-specific power modules.

- **FY14 Specific Objective**

➢ Develop integration technologies and fabricate all SiC power modules for inverter/converter (one-, two-, and three-phase leg, 100A/1200V rated) with lower thermal resistance, small electrical parasitic parameters, enabling exploitation of WBG superior attributes.

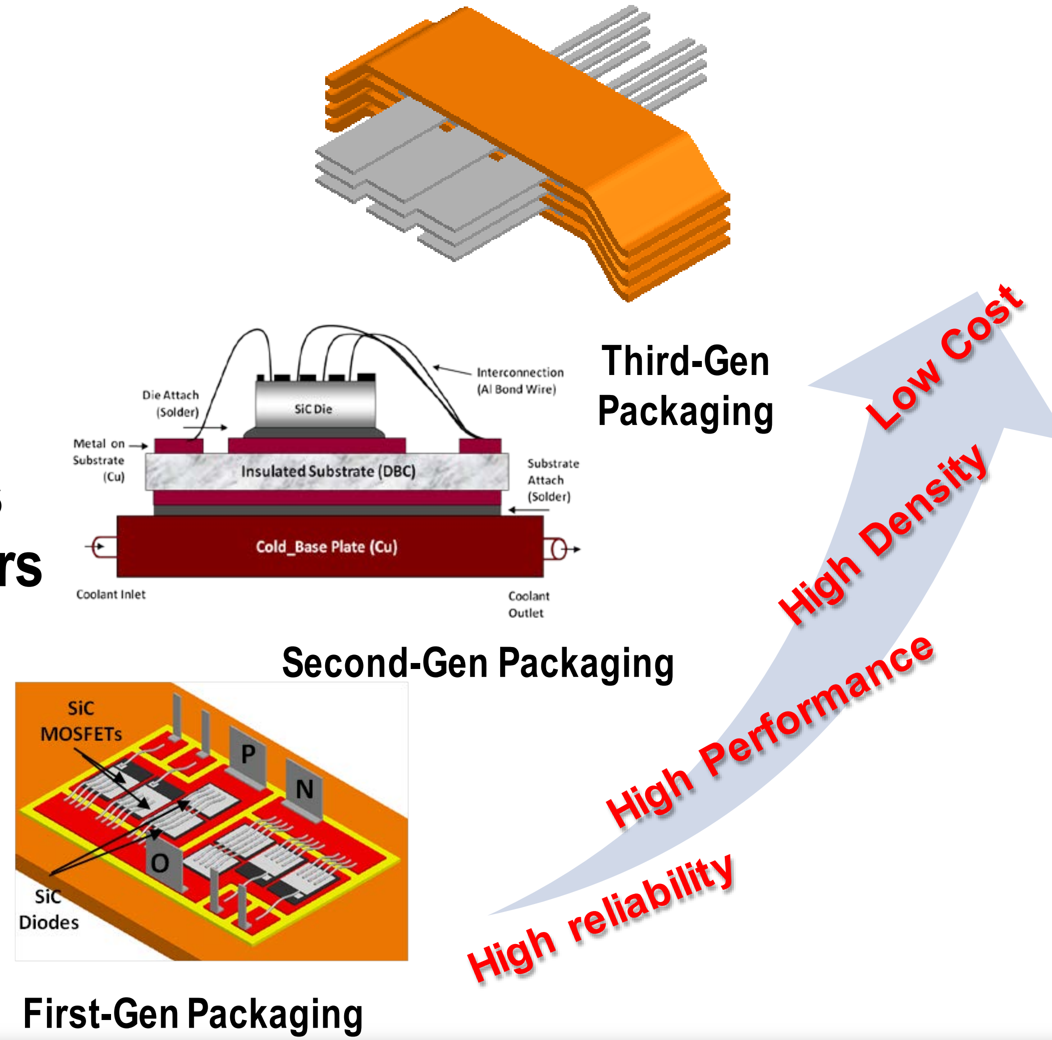
➢ Integrate WBG power modules to ORNL APEEM inverter/converter for improvements with 40% cost reduction and 60% power density increase of the power modules.

Milestones

Date	Milestones and Go/No-Go Decisions	Status
Sept-2013	Milestone: -Develop advanced All-SiC phase leg power module rated at 100A/1200V prototypes	Completed (1st-, and 2nd-Gen) phase-leg prototypes and evaluated at module- and converter-level
Sept-2013	Go/No-Go decision: -Determine if WBG modules can meet the APEEM targets on cost and power density	Shown promise to meet the APEEM targets
Dec 2013	Milestone: -Develop an advanced design of WBG integrated power module for inverters, converters, and chargers	Completed (a 3rd-Gen packaging invention disclosure filed)
June-2014	Go/No-Go decision: -Determine if the developed power modules enable inverters to meet the APEEM targets in cost and power density, then optimize the design accordingly	On Track - Prototypes will be fabricated and evaluated

Approach/Strategy

- Replace Si devices with their SiC and GaN counterparts to promote their accelerated adoption in traction drive systems
- Develop innovative power packaging techniques to exploit the superior attributes of WBG power semiconductors
  - High voltage, high current density
  - High frequency
  - High temperature

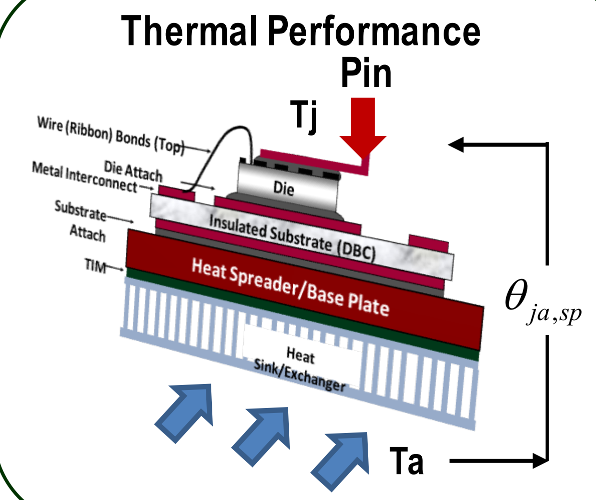


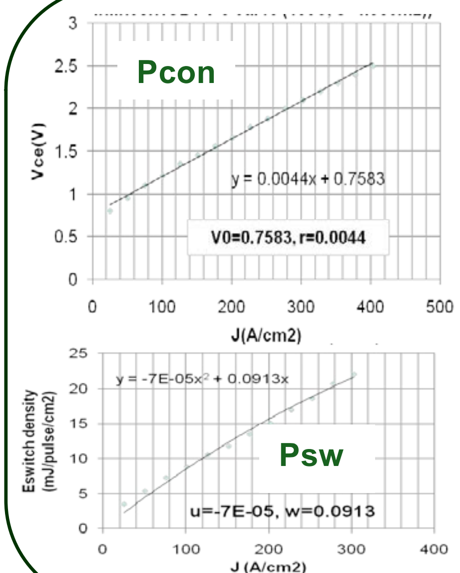
Approach/Strategy: Technology Advancement

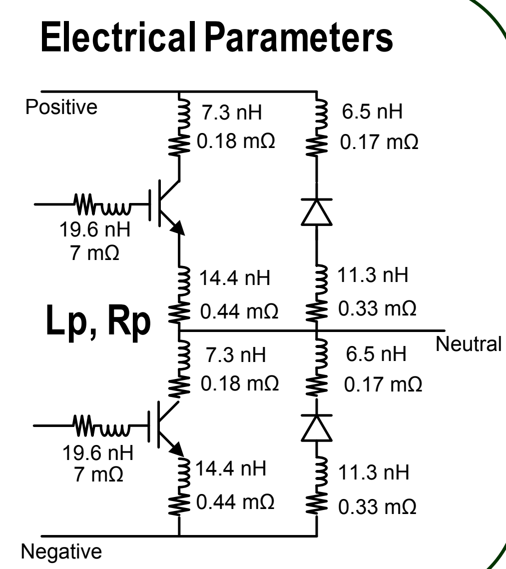
Life Time $\rightarrow N_f = \alpha \cdot \left(\frac{1}{Tj - Ta}\right)^{\beta} \cdot \exp(E_a / kT_m)$

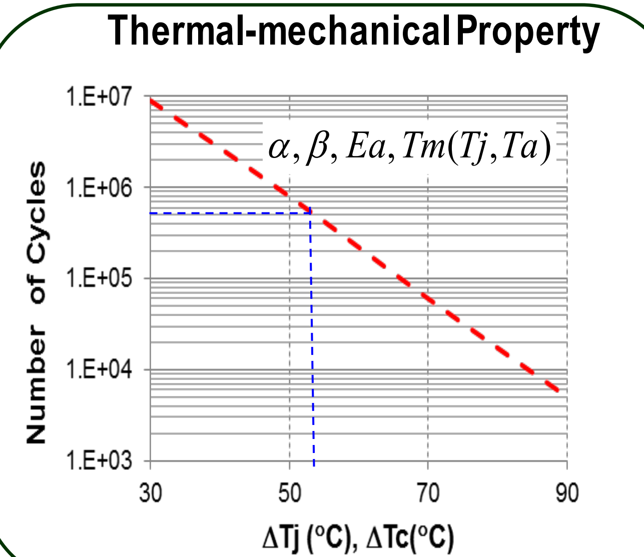
Efficiency $\rightarrow \eta = 1 - (Pcon + Psw + P_{lp} + P_{Rp}) / Pin$

Cost $\rightarrow \frac{\$}{kW} = A + B \cdot \frac{(1-\eta)\cdot\theta_{ja,sp}}{(T_j - T_a)}$ **Manufacture + Semiconductors**

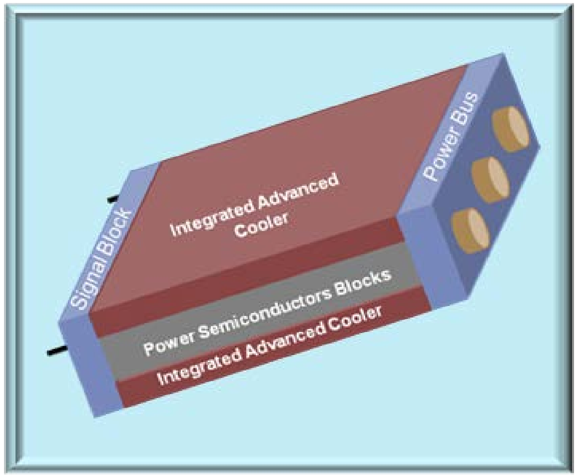




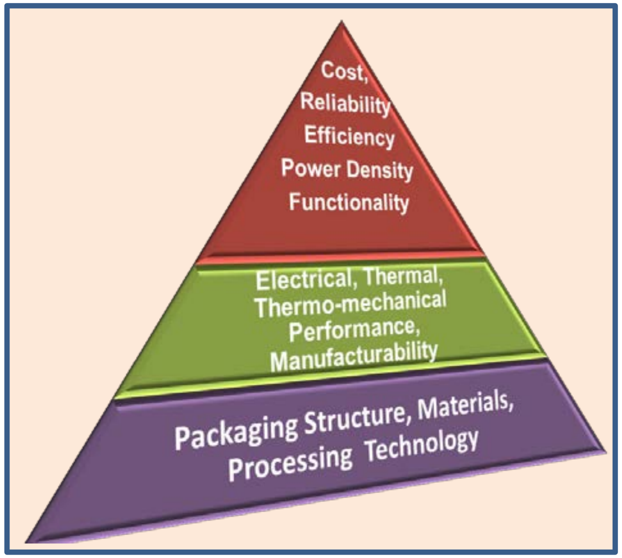




Approach/Strategy

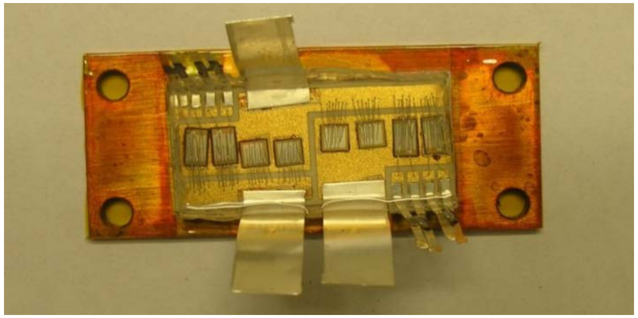


Advanced WBG Power Module

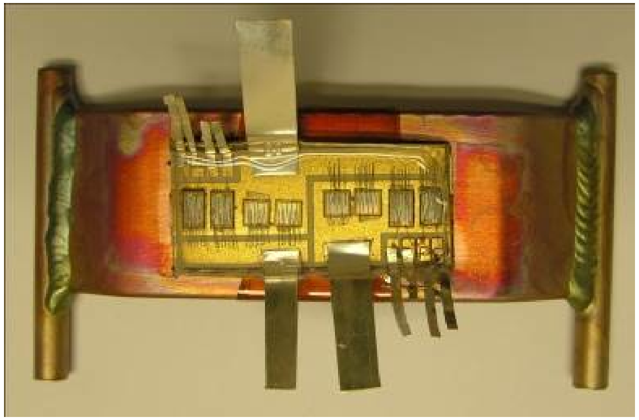


- ❑ 3-D Electrical Interconnection,
- ❑ Highly Efficient Heat Transfer
- ❑ High Temperature CTE Matched Materials and Processes
- ❑ Comprehensively Optimized Structure
- ❑ Low Cost Manufacturability

Technical Accomplishments and Progress
Completed 1st- and 2nd - Gen SiC Packaging-FY13

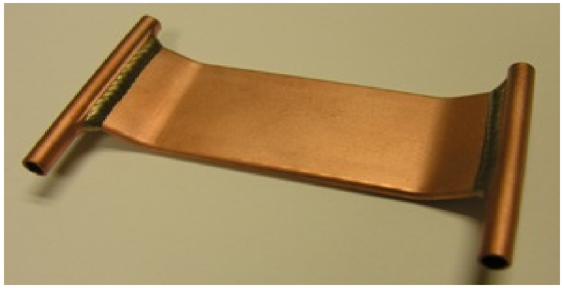


1st–Gen 100A/1200V Phase-leg Module



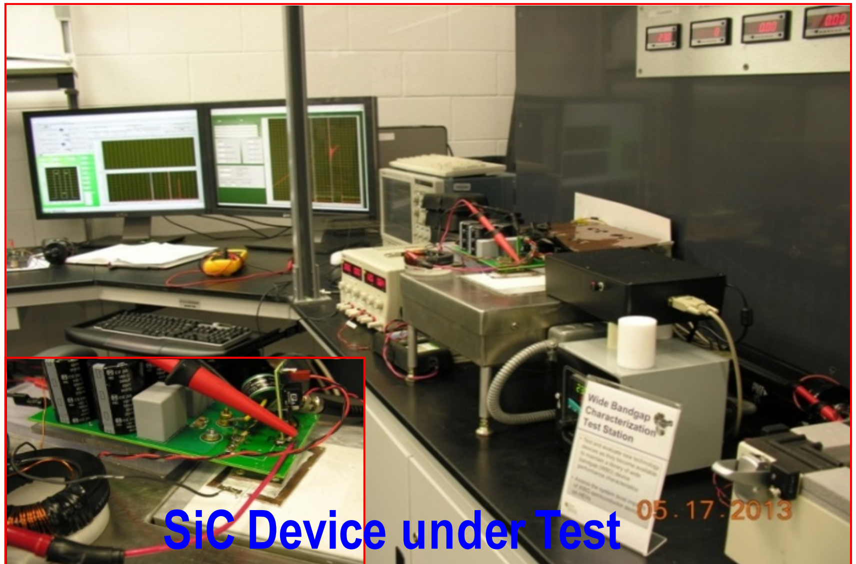
2nd–Gen 100A/1200V Phase-leg Module

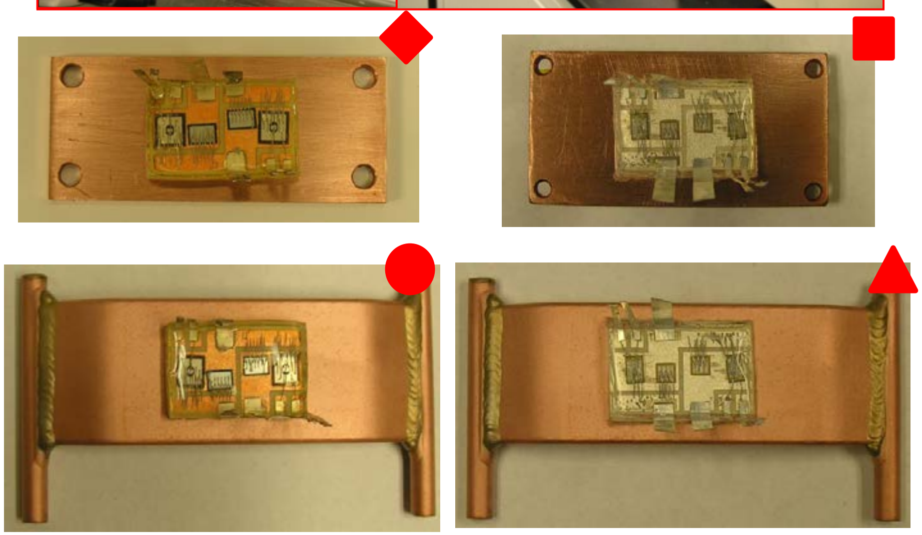
Conventional Baseplate in the 1st-Gen Module



Integrated Cold Plate in the 2nd-Gen Module

Technical Accomplishments and Progress
Evaluated the Packaging Prototypes-FY13

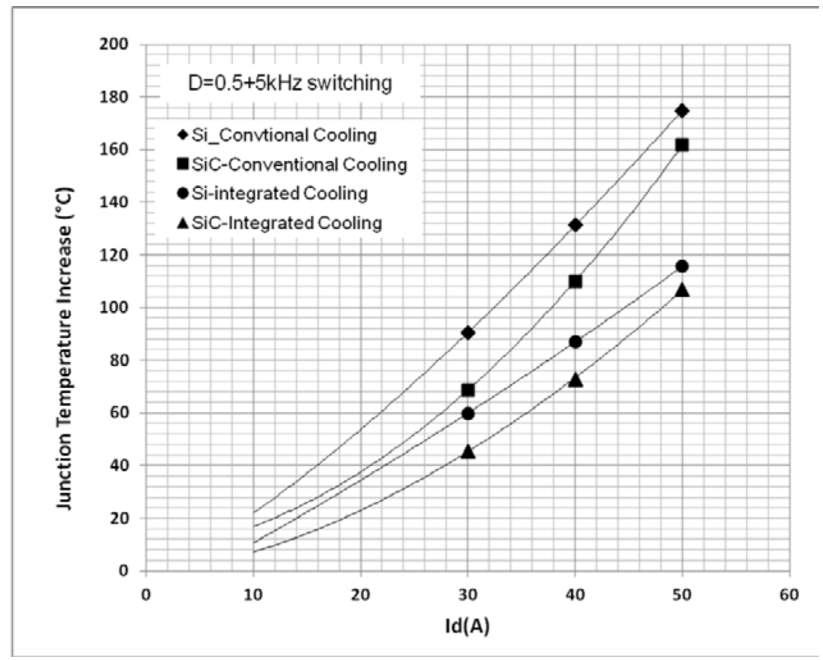




Photographs of Four Device/Package Combinations

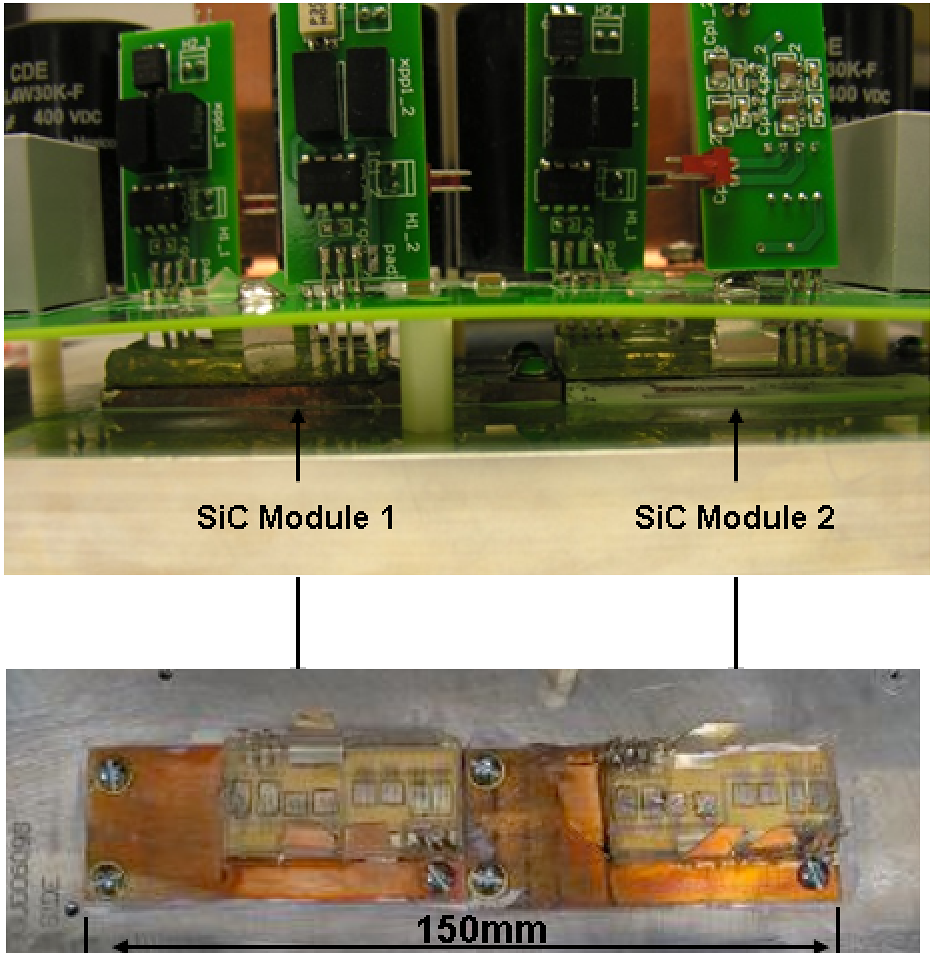
Current Density Allowed at ΔTj=100°C for a Typical Operation

Item	Si_Con. Cooling	SiC_Con. Cooling	Si_Integ. Cooling	SiC_Integ. Cooling
Current Density J_d (A/cm^2)	◆ 65.35	■ 144.97	● 97.57	▲ 184.98

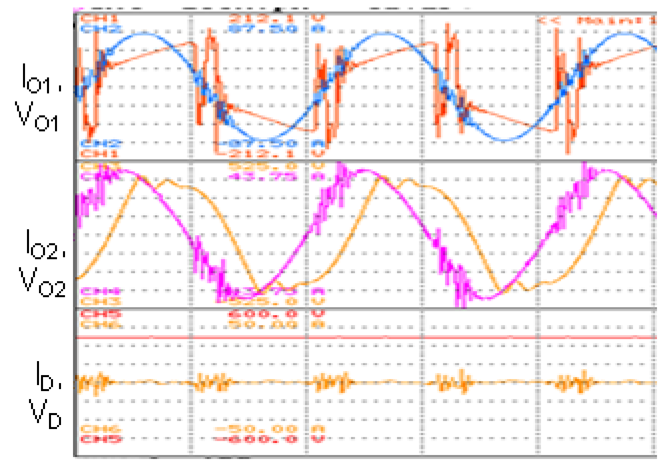


Junction Temperature vs Current for Different Packages

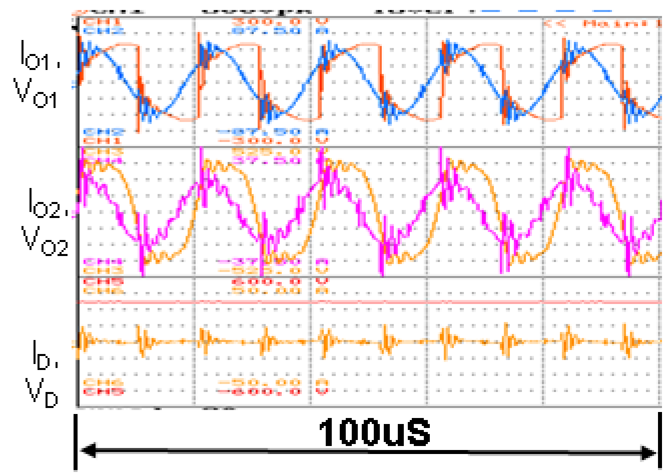
Technical Accomplishments and Progress
Evaluated SiC modules in converter-FY13



Two 100A/1200V SiC Power Modules in a HF converter (liquid cooled)

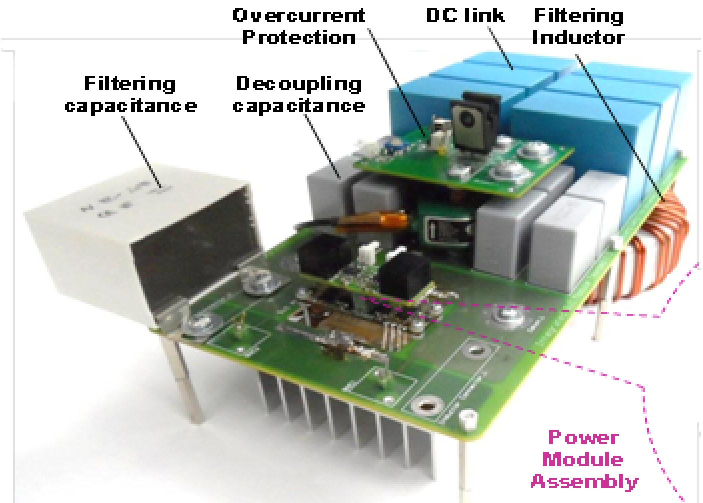


Waveforms at 24KHz, 3.5kW Switching

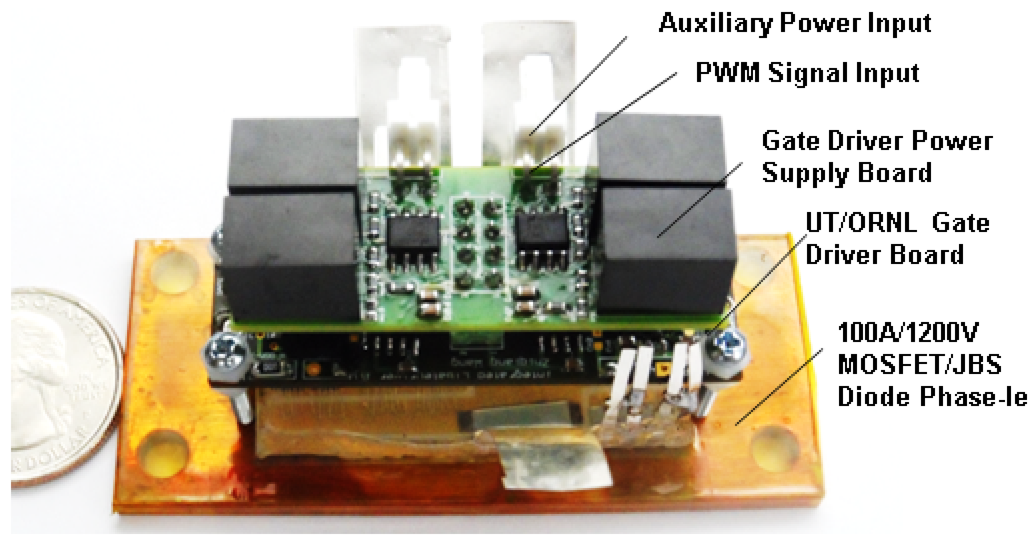


Waveforms at 48 KHz, 3.5 kW Switching

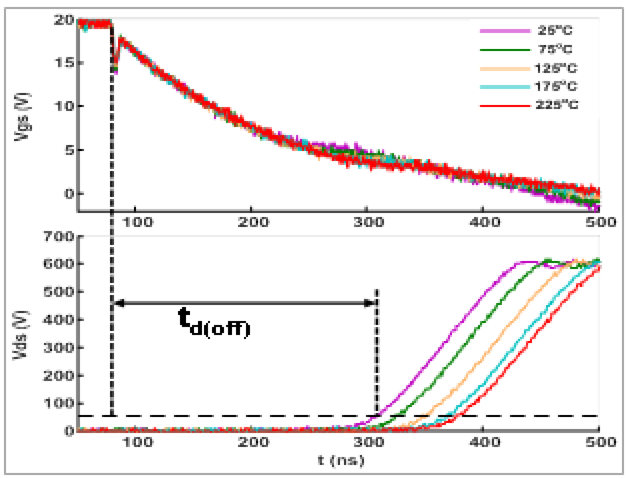
Technical Accomplishments and Progress
Packaged SiC IPM and Evaluation-FY13/14



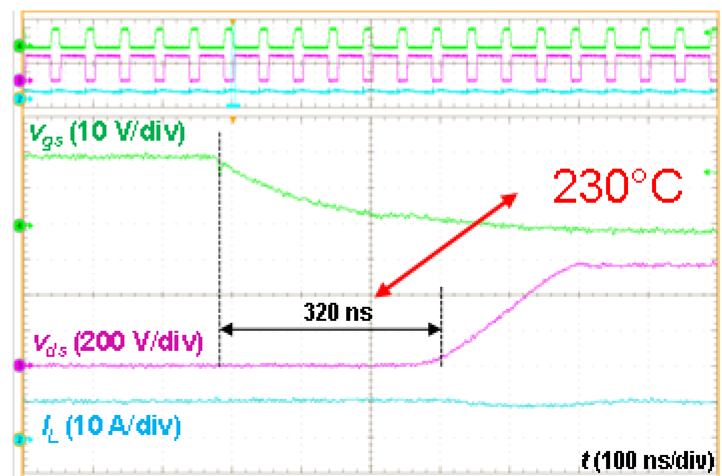
Forced Air Cooled Buck Converter
600V/150V, 10A, up to 100kHz



SiC Integrated Power Module (IPM)



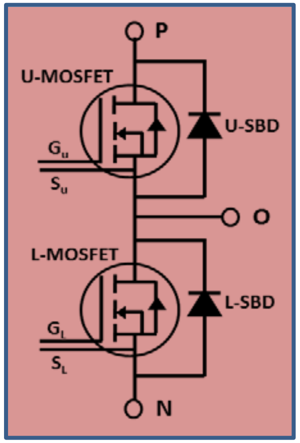
Calibration of turn-off delay time vs temperature

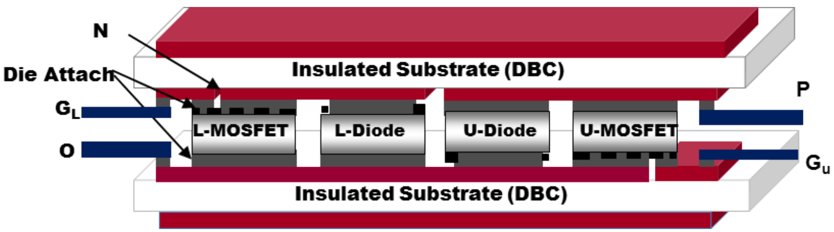


Waveforms at 100 KHz, 600V/ 150V, 10 A Switching

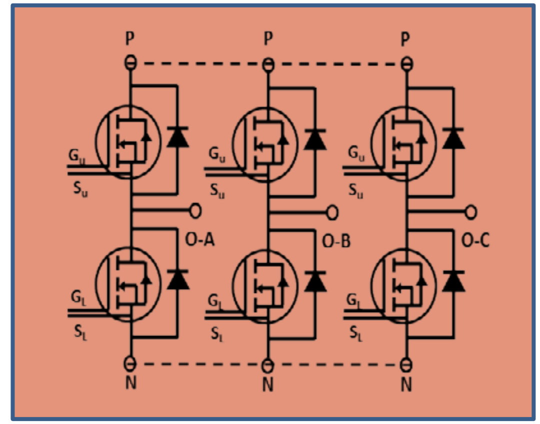
Technical Accomplishments and Progress

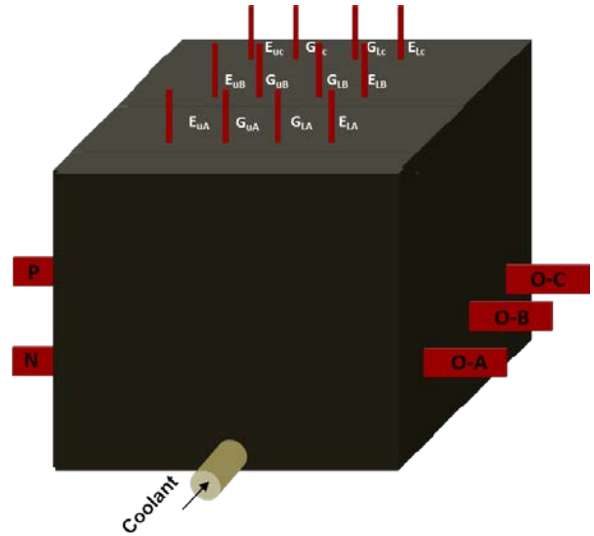
Completed 3rd-Gen Packaging Design-FY14





Planar-Bond-All (PBA)
Single Phase-leg Unit

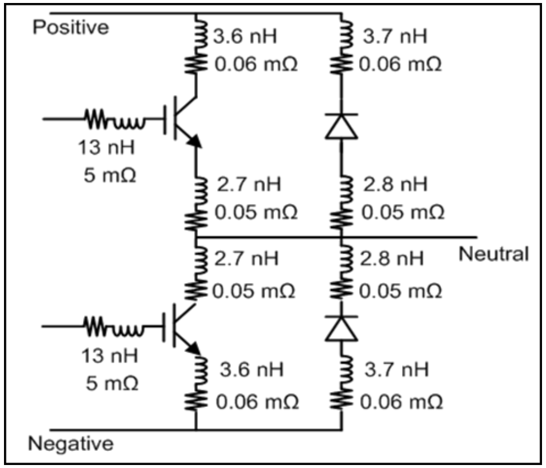




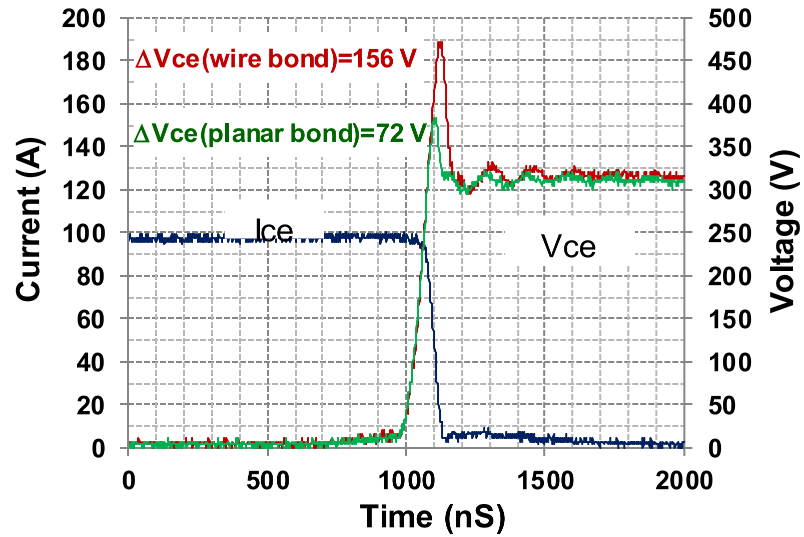
Integrated Multi-Phase-leg Assembly

Technical Accomplishments and Progress

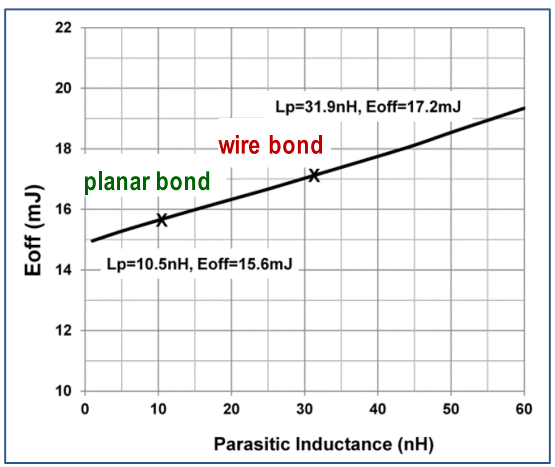
Evaluated Electrical Performance-FY14



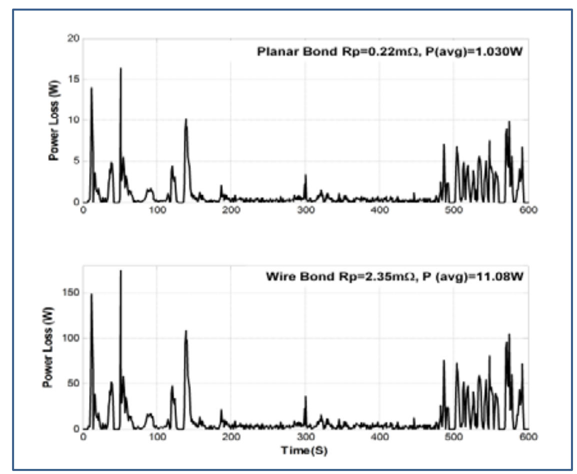
Electrical Parasitic Parameters



Switching Ringing due to Parasitic Inductance

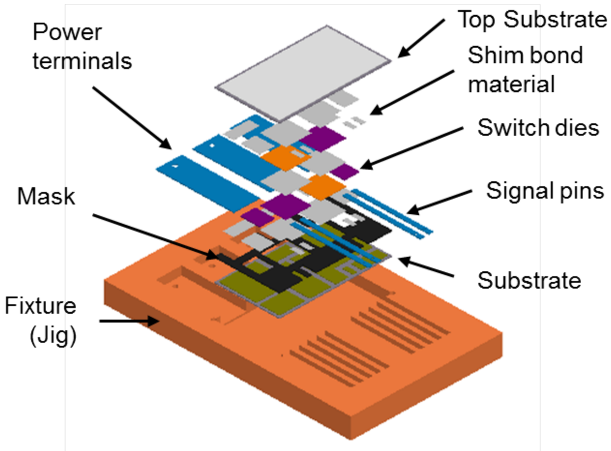


Switching Power Loss due to Parasitic Inductance

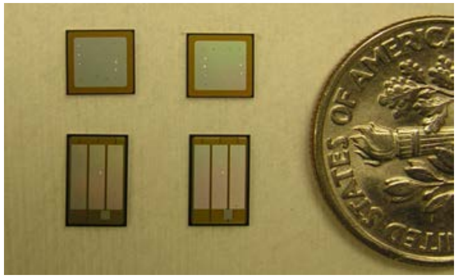


Power Loss due to Parasitic Resistance

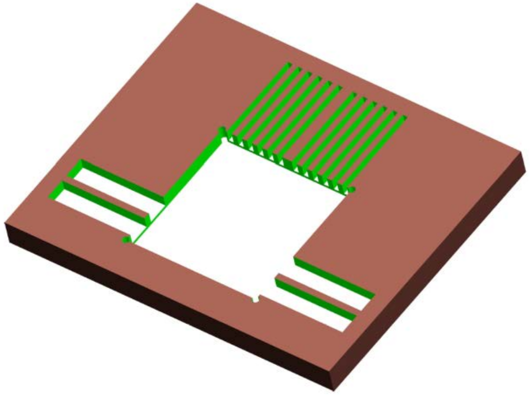
Technical Accomplishments and Progress
Completed Components and Tools-FY14



Planar Bond All (PBA) Process



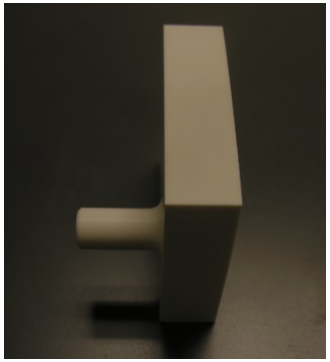
Specialized SiC Devices



Fixture (Jig)

Top and Bottom Substrates

Cold-plates



Coolant Manifold

* Invention Disclosure 201303211, DOE S-124,816

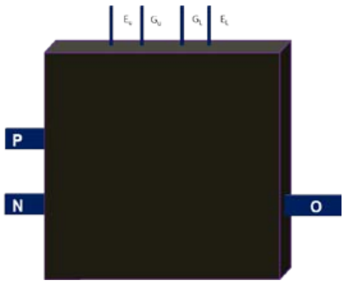
Responses to Previous Year Reviewers' Comments

- **Recommendation/Comment:**
  Is double sided cooling planned for a future generation?
- **Response/Action:**
  Yes, the double sided cooling concept has been incorporated in the 3rd –Gen packaging design (FY14).
- **Recommendation/Comment:**
  It may be better to expand on NREL's work than to start from scratch on another reliability assessment.
- **Response/Action:**
  The new power module reliability will be done in collaboration with NREL.
- **Recommendation/Comment:**
  There is no industry or other DOE laboratory collaborators that are part of the team.
- **Response/Action:**
  The roles and activities have been clarified that we worked together with industry and other DOE labs.

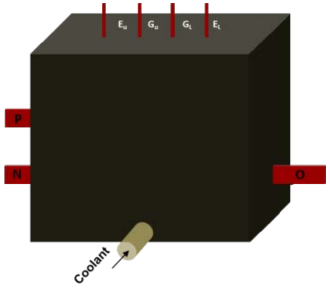
Collaboration and Coordination

Organization	Type of Collaboration/Coordination
CREE	Design and fabricate ORNL specific SiC MOSFET and diode dies
U.S. DRIVE EETT members	Discuss and refine the technical specifications with OEMs
Remtec	Co-design and manufacture packaging components
Fralock	Co-design and fabrication specialized package parts
Cool Innovations	Co-design and supply specialized package parts
NREL	Thermal analysis of an ORNL designed package
ORNL MSTD/DOE VTO Propulsion Materials Program	Packaging materials characterization
University of Tennessee at Knoxville	Module performance characterization

Proposed Future Work
Remainder of FY14



- Complete prototyping of designed SiC PBA power modules
  - Perform complete packaging processes for manufacture of modules
  - Complete electrical, thermal characterization of prototypes



- Provide APEEM converter/inverter research teams
  - Manufacture various types of prototype modules: integration of double sided cooling into SiC converter modules
  - Perform comprehensive comparison of electrical, thermal, and thermo-mechanical performance of prototypes
  - Calculate system’s cost, density, etc.

Proposed Future Work
FY15 and Beyond

- **Complete packaging integration of intelligent WBG power modules**
  - Incorporate ORNL advanced high temperature gate drive circuitry
  - Implement high temperature multi-chip module cooling technologies
  - Optimize interconnection layout between control/drive and WBG power stage
- **Enhance reliability of and optimize the 3rd-Gen WBG power packaging design**
  - Incorporate ORNL advanced bonding material/processing, encapsulate, thermal materials
  - Perform thermo-mechanical design and simulation of advanced module packages
  - Implement cost-effective materials and structures into WBG power modules
  - Conduct simulation and preliminary reliability study of packages
- **Provide packaging support for other APEEM projects**
  - Deliver advanced customer-specific prototypes to APEEM team for WBG power electronics systems development
- **Commercialization of developed technologies**
  - Work together with industry to transfer the technologies to manufacturers

Summary

- **Relevance:** Focused on achieving 40% cost reduction and 60% power density increase to facilitate DOE APEEM 2020 power electronics targets: \$3.3/kW, 14.1kW/kg, 13.4kW/L.
- **Approach:** The 3rd-gen WBG packaging technology being developed is to leapfrog barriers of existing industrial baseline and bring innovative, systemic development to advance technologies.
- **Collaborations:** Latest industrial products and universities' advanced research have been incorporated in the project. The achievements of this work are efficiently transferred to the industry through collaborations.
- **Technical Accomplishments:**

  Developed application specific WBG modules for system evaluation:
  - The 2nd –gen All-SiC 100A/1200V phase-leg modules delivered for system evaluation;
  - An innovative 3rd- gen planar-bond-all (PBA) SiC package has been designed and fabrication and evaluation of the module prototypes are on track;
  - SiC power devices compared to Si ones: 55% die size, 60% conduction power loss, 20% switching power loss.
  - New packaging (relative to industrial SOA): 35% thermal resistance reduction, 75% inductance decrease, 80% resistance reduction, 30% overall volume and weight reduction.
- **Future Work:** Continue to optimize the technologies and work together with industry to transfer them to manufacturers.